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9623448	25.06.1996	

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(52) UK CL (Edition O)
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Research Disclosure 38337, 10/3/96. Patent Abstracts of Japan, Section C, Section No 307, Vol 9, No 247, Pg 114, 3/10/85 & JP60-104129A Patent Abstracts of Japan, Section P, Section No 87, Vol 5, No 173, Pg 45, 5/11/81 & JP56-100350A

(58) Field of Search
UK CL (Edition O) G5C CHG , H1K KCAA KJAD
INT CL[6] G02F 1/136 , H01L
Online:WPI, JAPIO, CLAIMS, EDOC, INSPEC

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Jeong-Hyun Kim

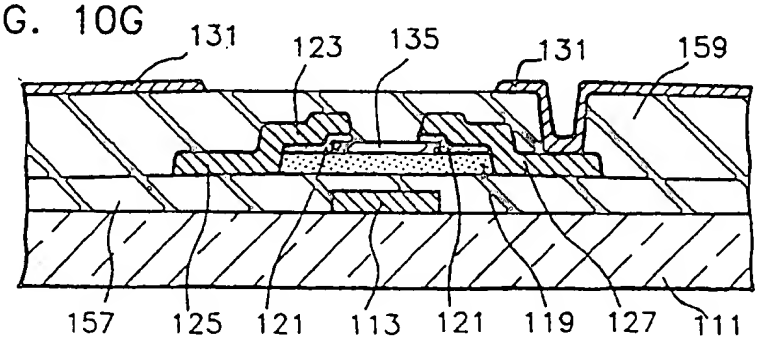
(72) cont
Woon-Kwon Kim
Ki-Hyun Lyu

(74) continued overleaf

(54) Liquid crystal display and method of manufacture

(57) A thin film transistor substrate for a liquid crystal display includes a substrate (111); a thin film transistor over the substrate, the thin film transistor having a gate (113), a source (121, 123), a drain (121, 127), a semiconductor layer (119), and a gate insulation layer (157); and a protection film (159) over the thin film transistor, the protection film and/or gate insulation layer including a material derived from fluorinated polyimide, teflon (RTM), cytop (RTM), fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

FIG. 10G



GB 2 311 653 A

(74) Agent and/or Address for Service
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Chancery House, 53-64 Chancery Lane, LONDON,
WC2A 1SD, United Kingdom

FIG. 1 PRIOR ART

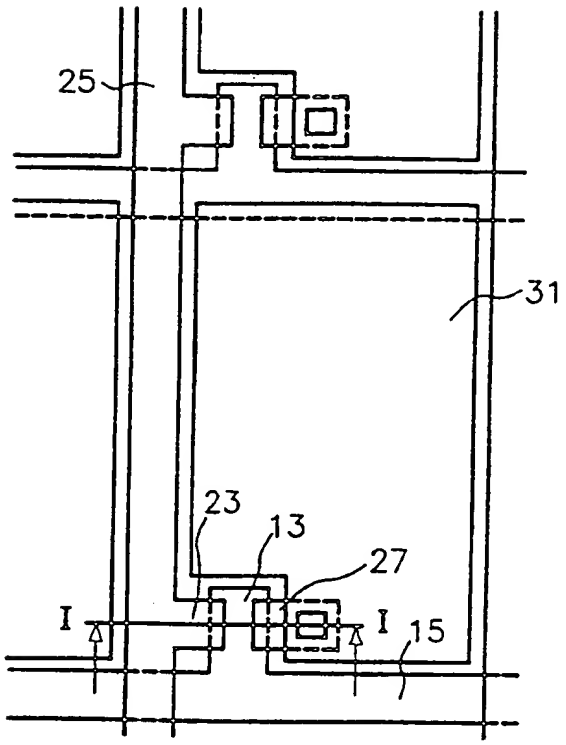


FIG. 6 PRIOR ART

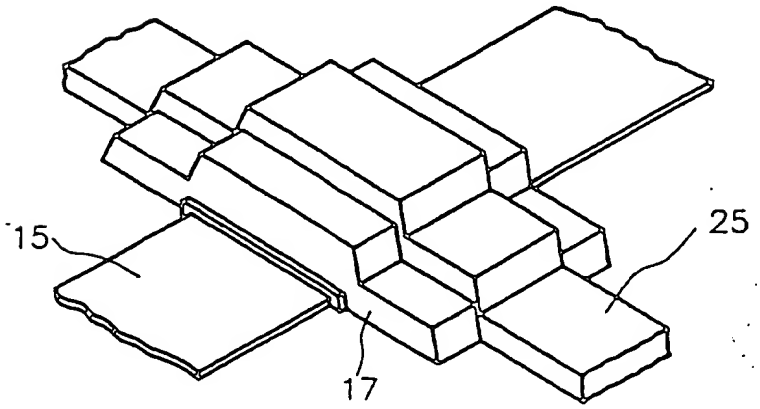


FIG. 2A PRIOR ART

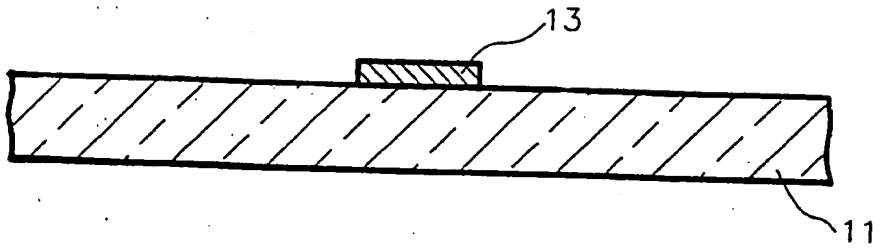


FIG. 2B PRIOR ART

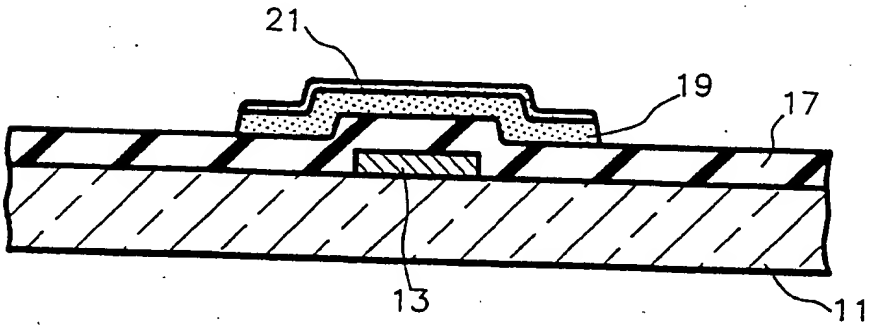


FIG. 2C PRIOR ART

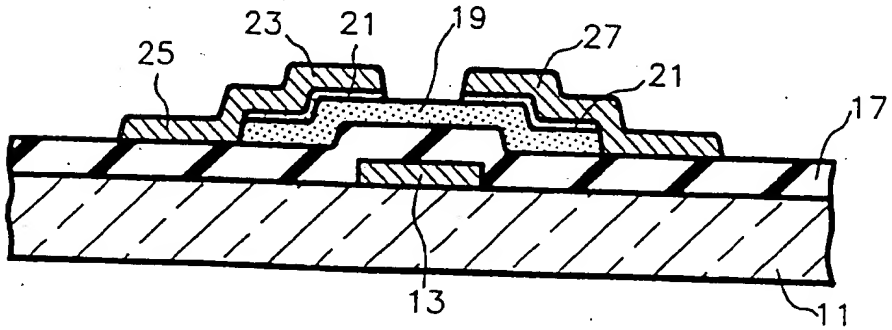


FIG. 2D PRIOR ART

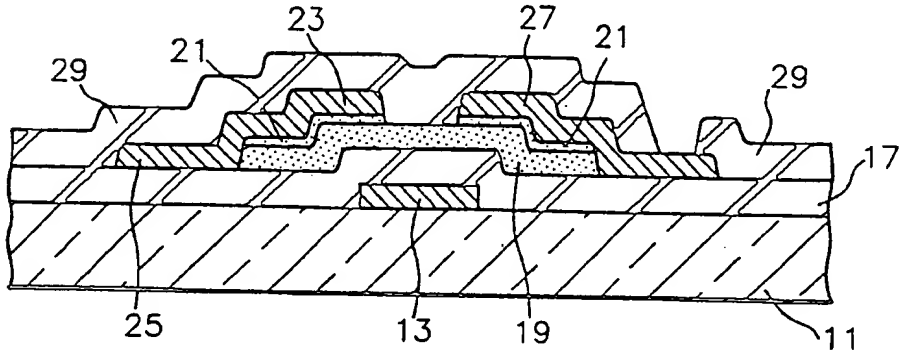


FIG. 2E PRIOR ART

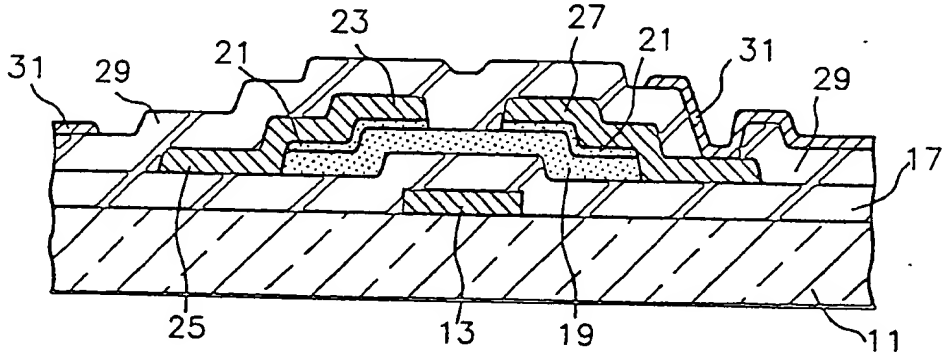


FIG. 2F PRIOR ART

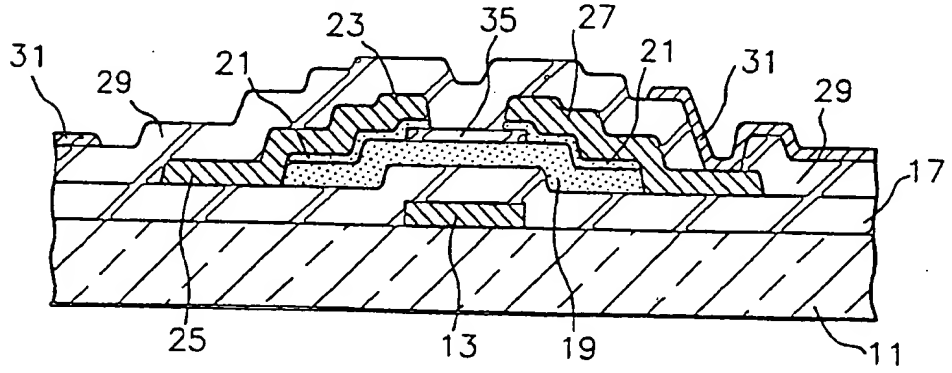


FIG. 3A
PRIOR ART

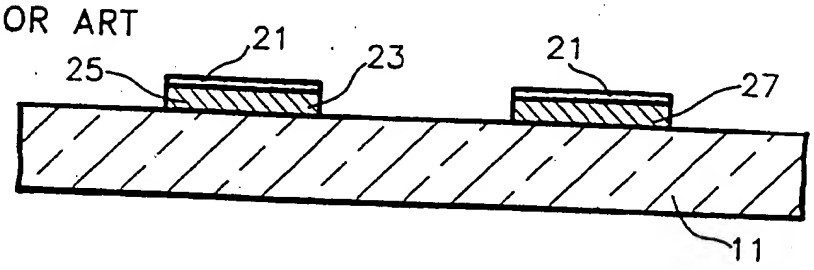


FIG. 3B
PRIOR ART

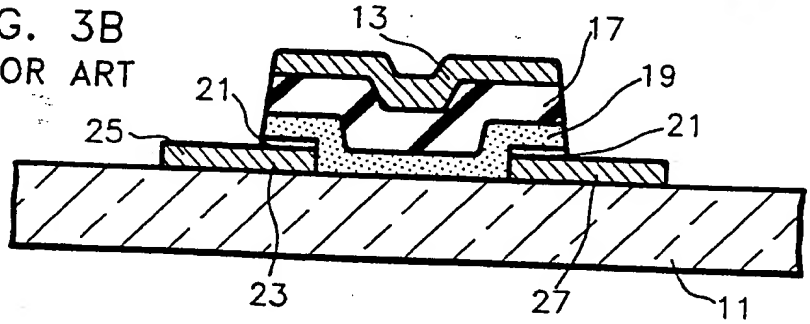


FIG. 3C
PRIOR ART

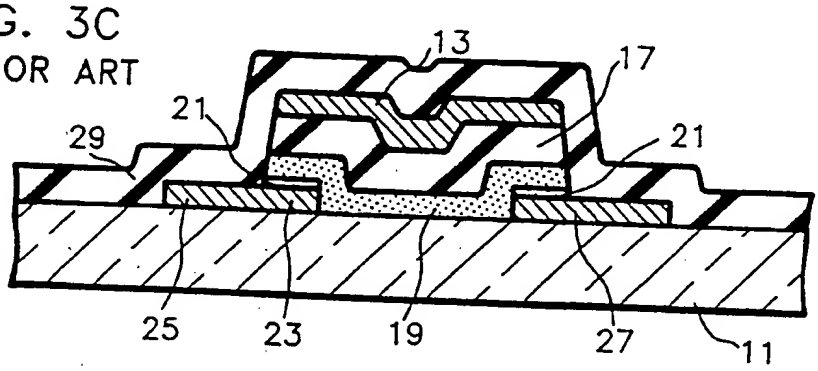


FIG. 3D
PRIOR ART

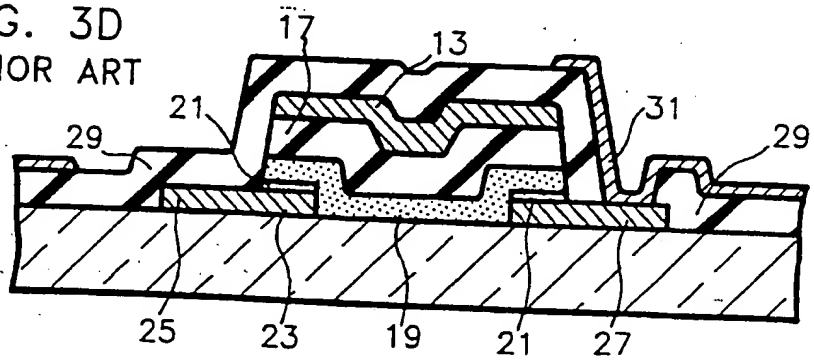


FIG. 4A
PRIOR ART

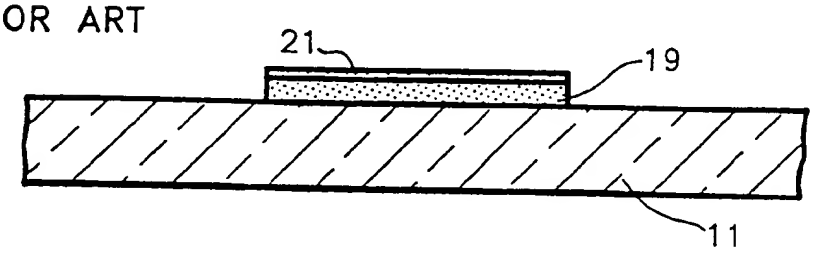


FIG. 4B
PRIOR ART

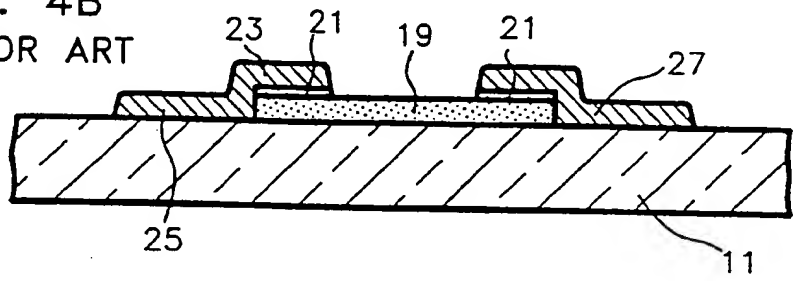


FIG. 4C
PRIOR ART

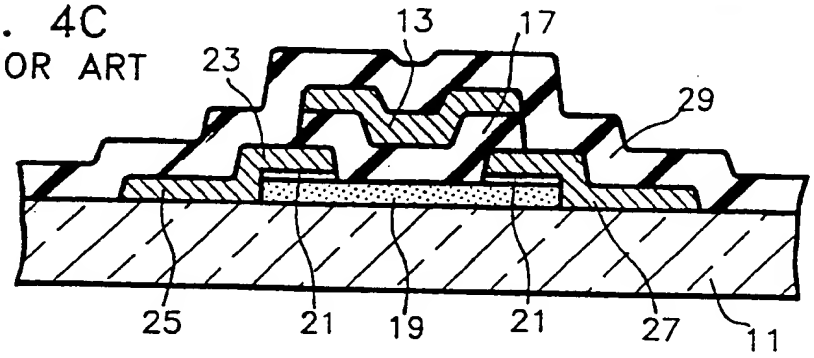


FIG. 4D
PRIOR ART

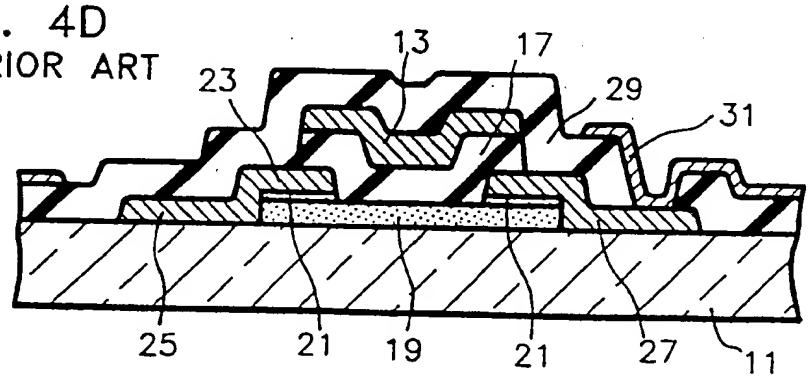


FIG. 5A
PRIOR ART

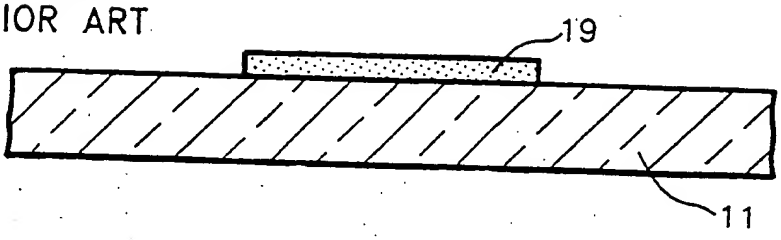


FIG. 5B
PRIOR ART

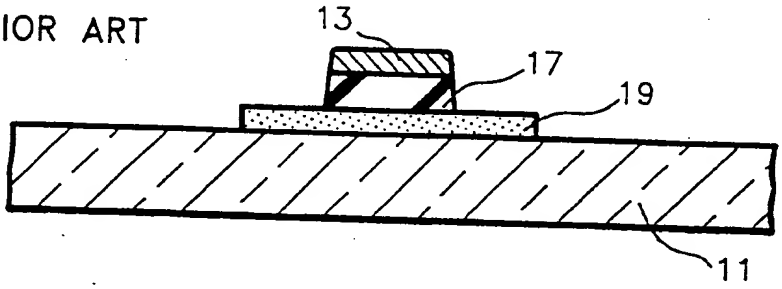


FIG. 5C
PRIOR ART

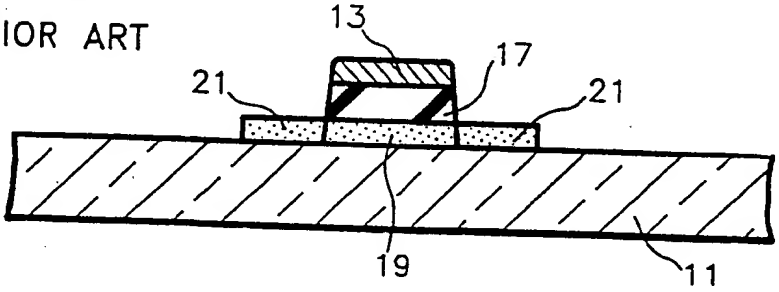


FIG. 5D
PRIOR ART

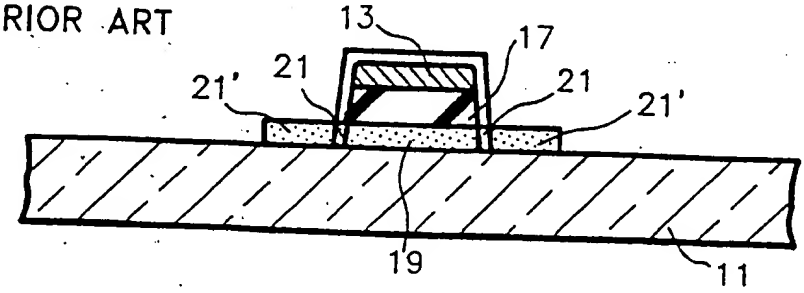


FIG. 5E
PRIOR ART

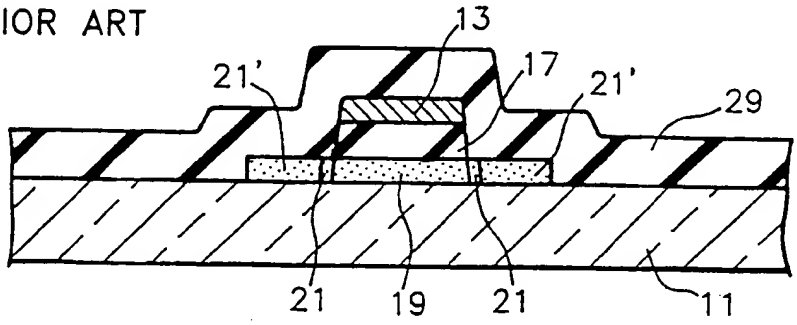


FIG. 5F
PRIOR ART

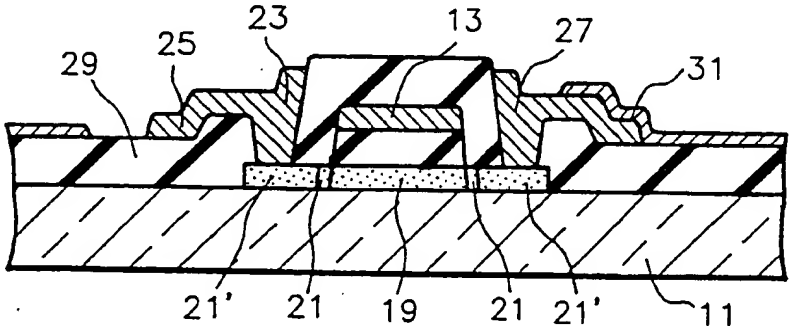


FIG. 5G
PRIOR ART

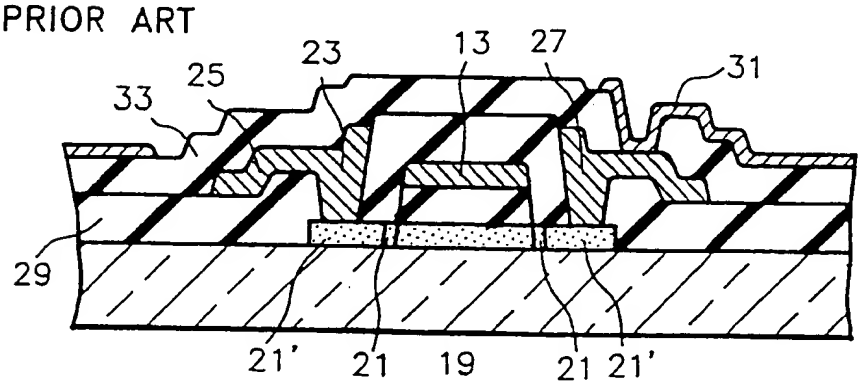


FIG. 7A
PRIOR ART

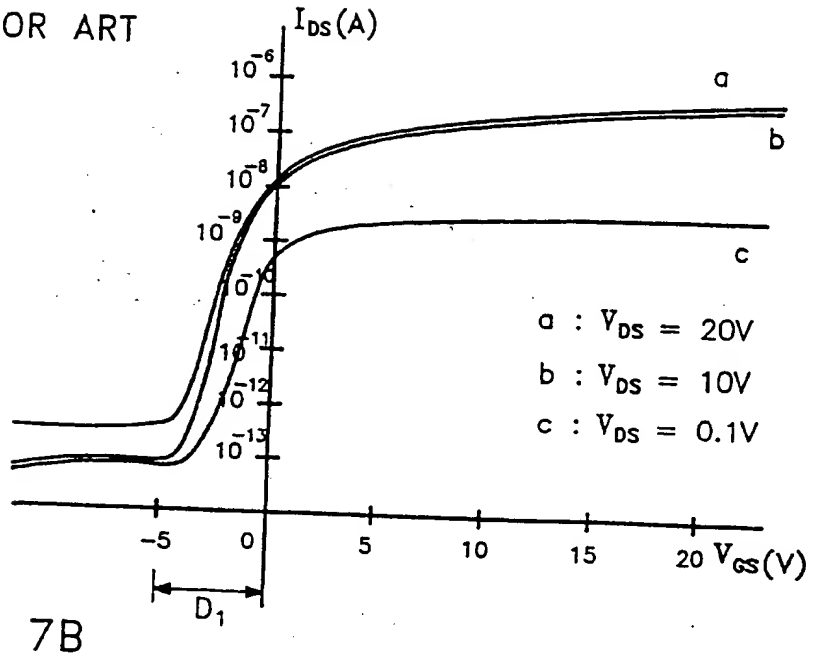


FIG. 7B
PRIOR ART

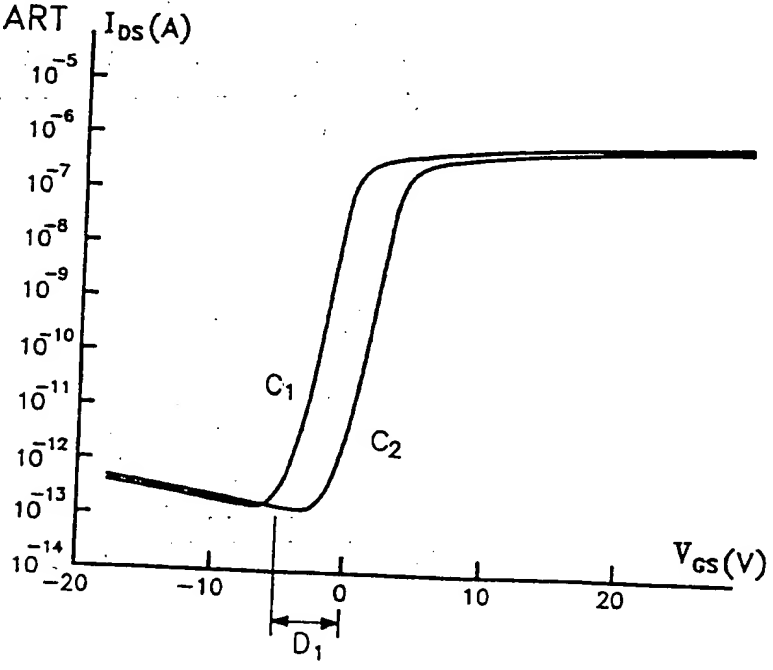


FIG. 8

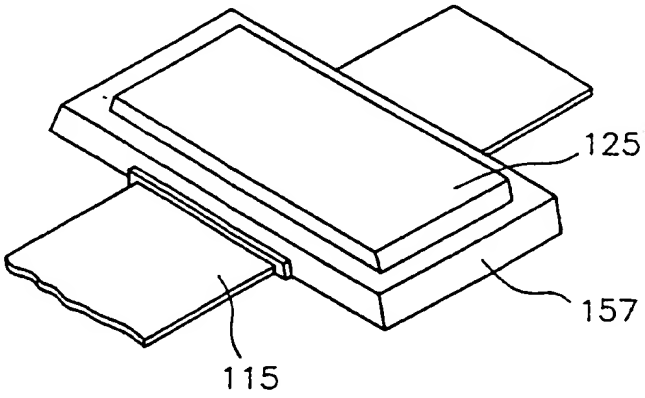


FIG. 9

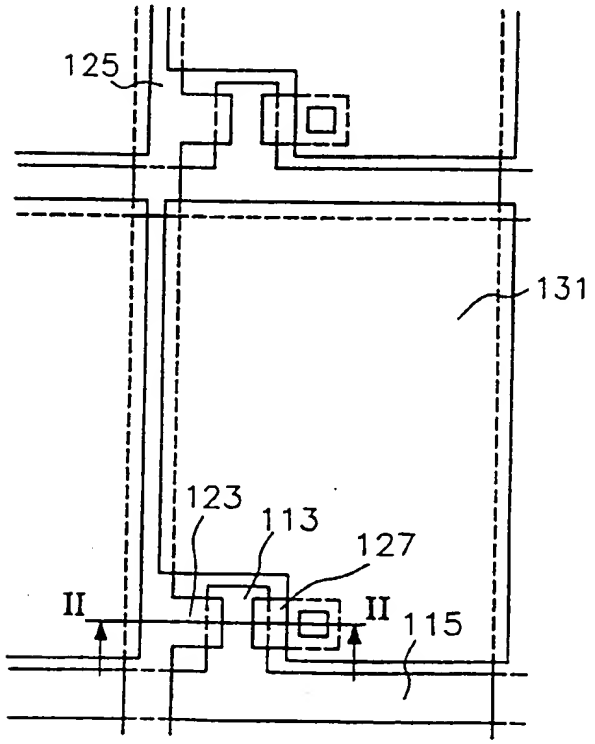


FIG. 10A

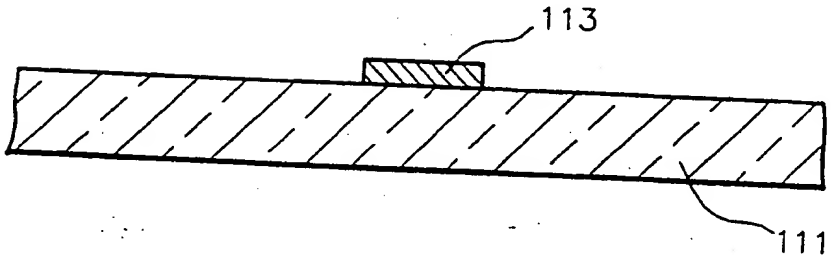


FIG. 10B

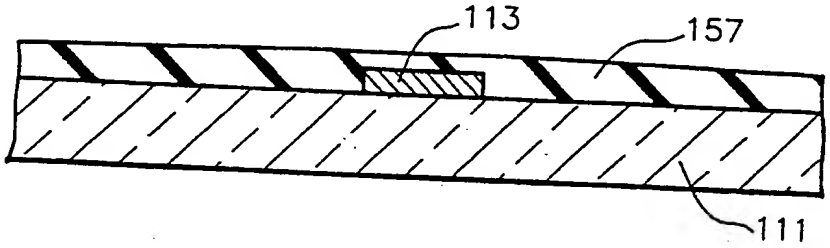


FIG. 10C

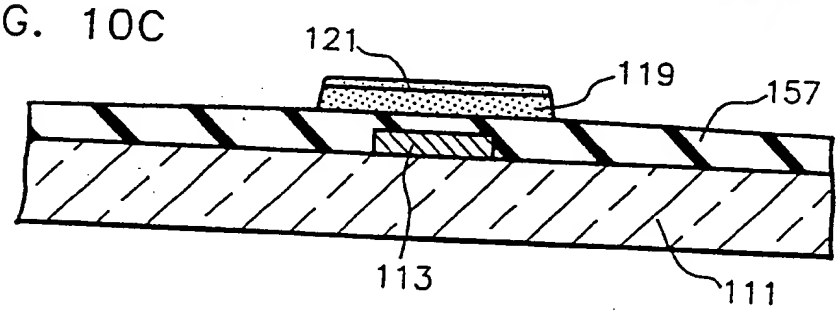


FIG. 10D

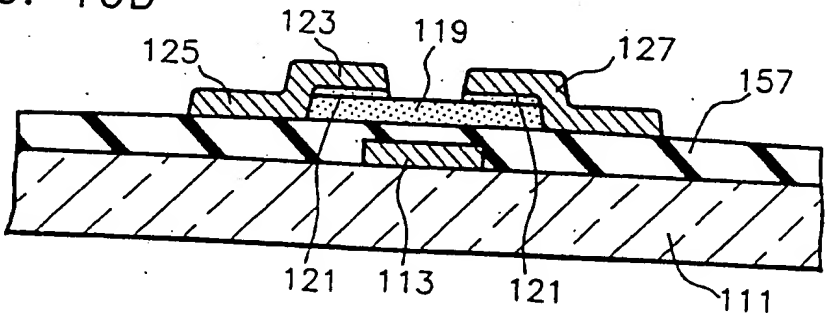


FIG. 10E

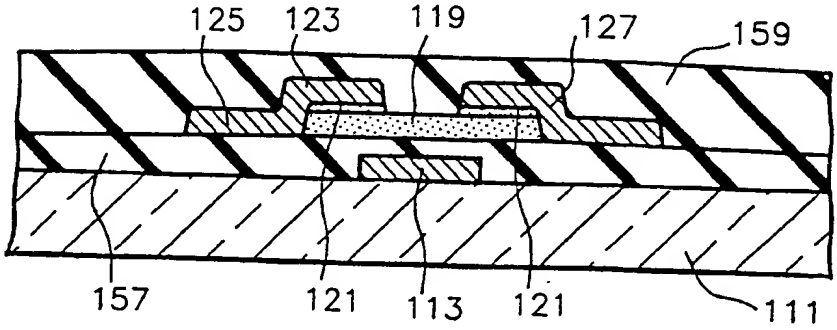


FIG. 10F

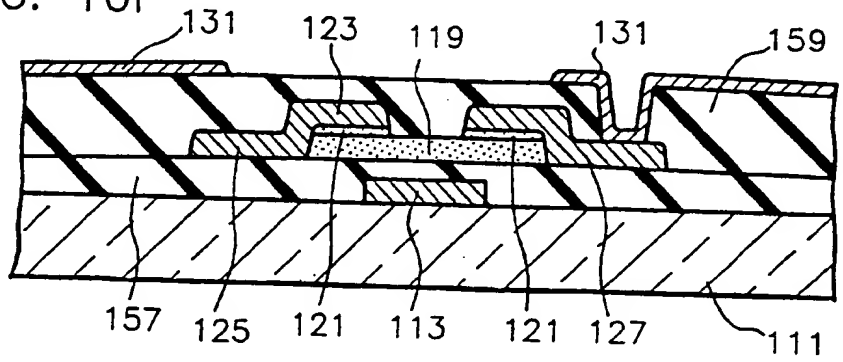


FIG. 10G

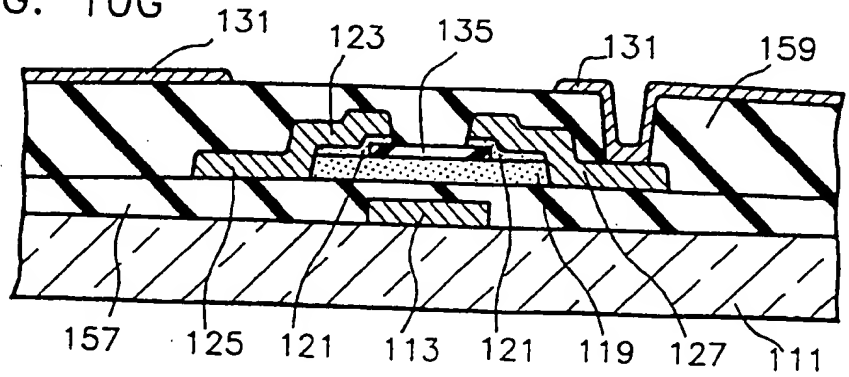


FIG. 11A

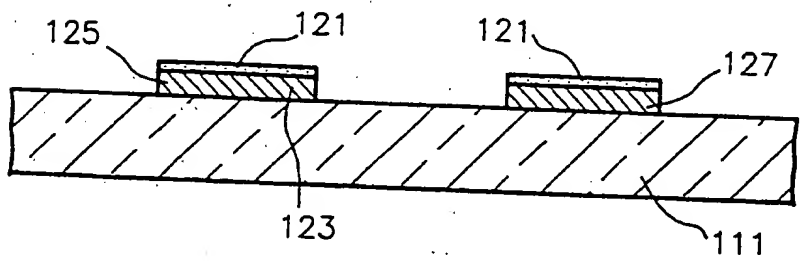


FIG. 11B

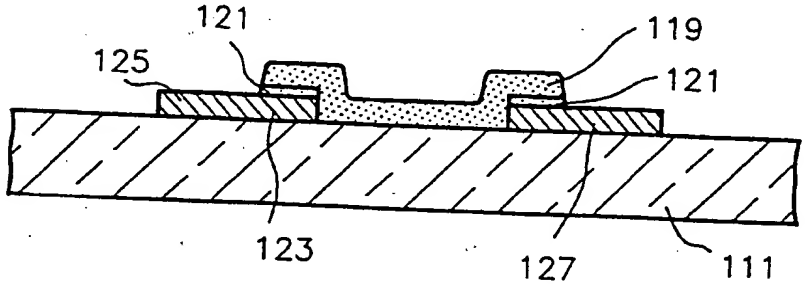


FIG. 11C

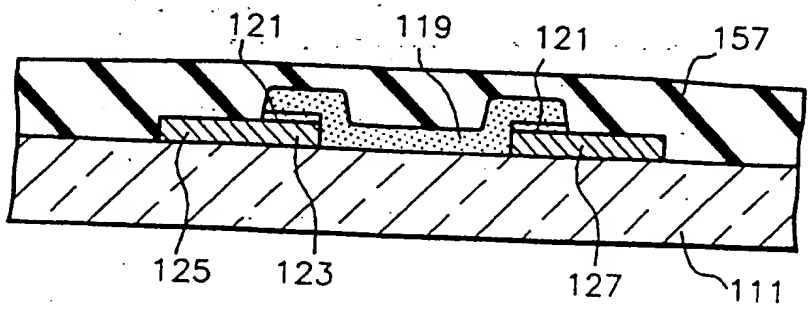


FIG. 11D

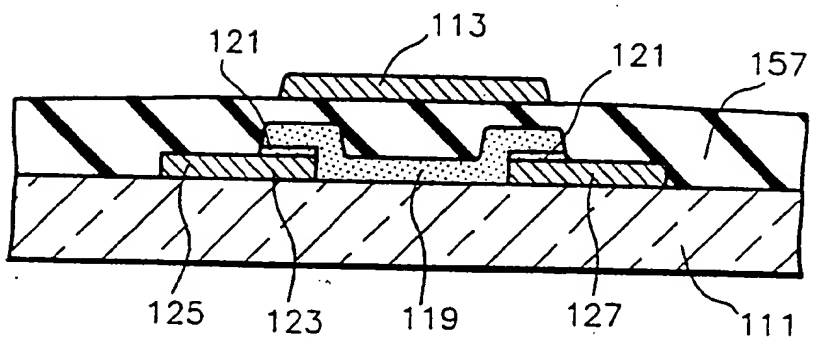


FIG. 11E

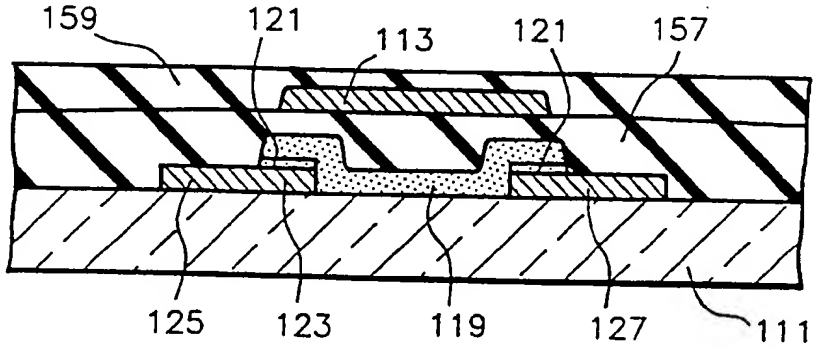


FIG. 11F

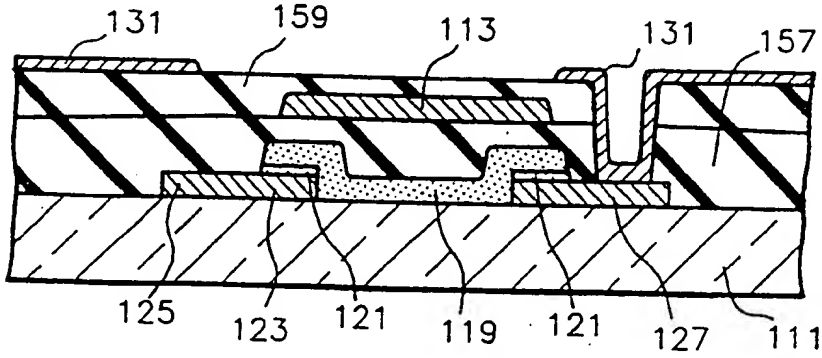


FIG. 12A

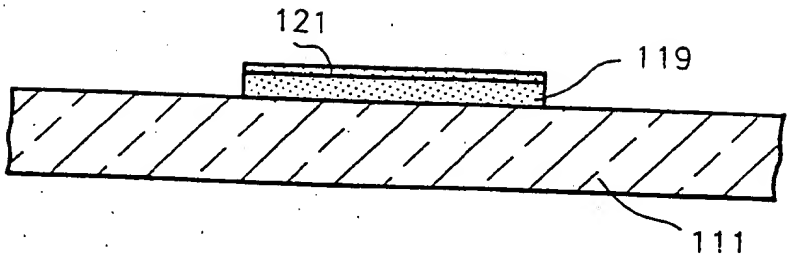


FIG. 12B

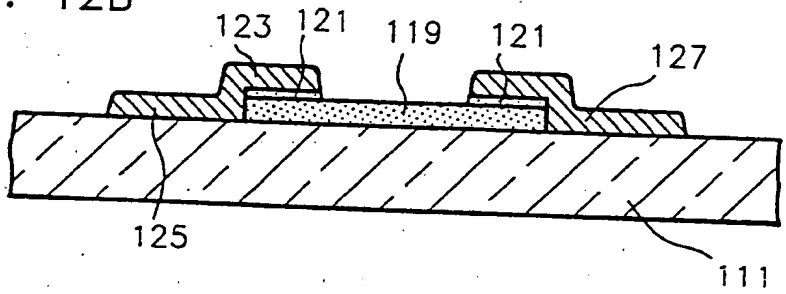


FIG. 12C

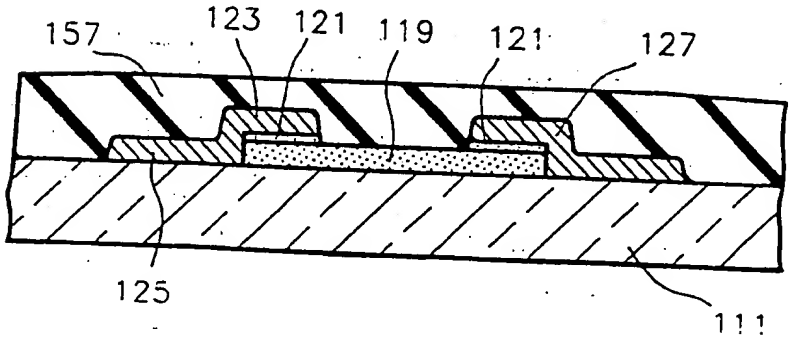


FIG. 12D

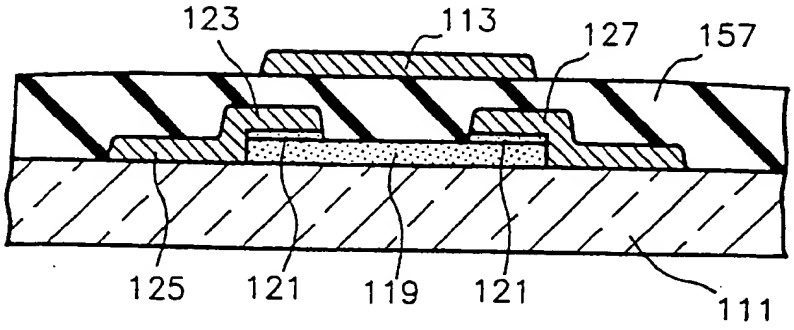


FIG. 12E

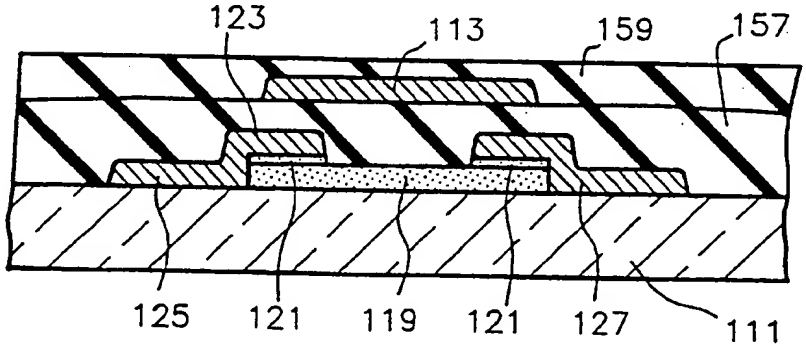


FIG. 12F

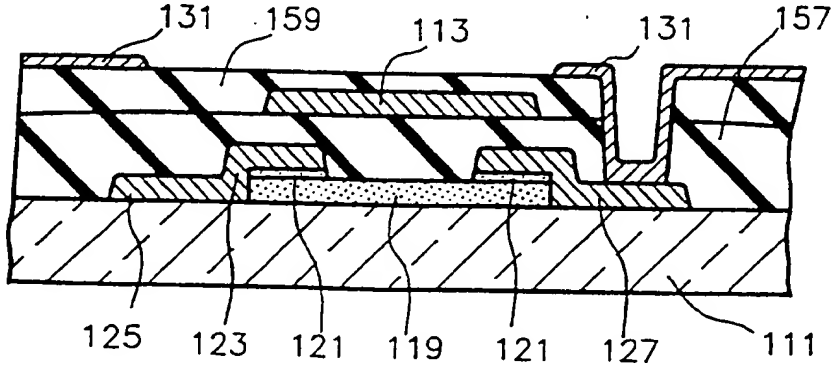


FIG. 13A

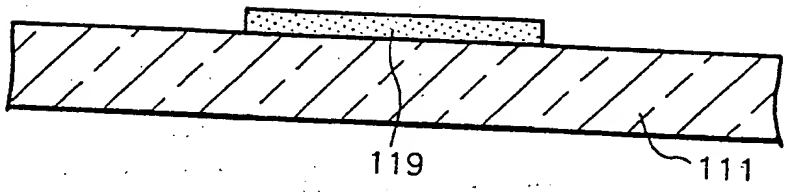


FIG. 13B

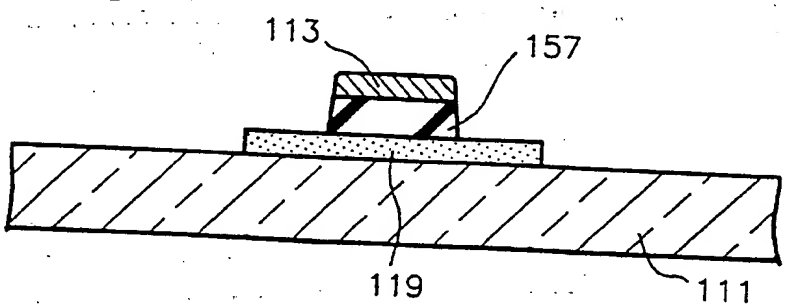


FIG. 13C

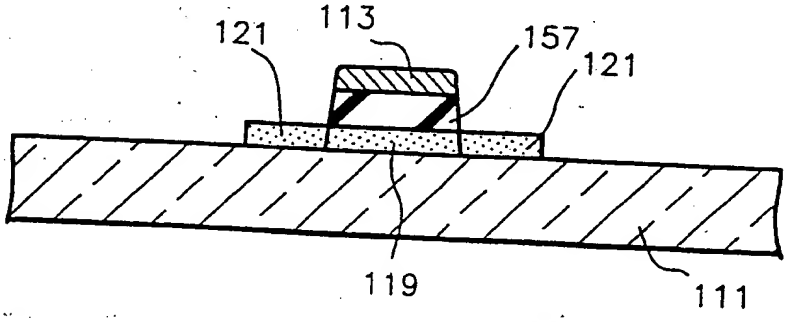


FIG. 13D

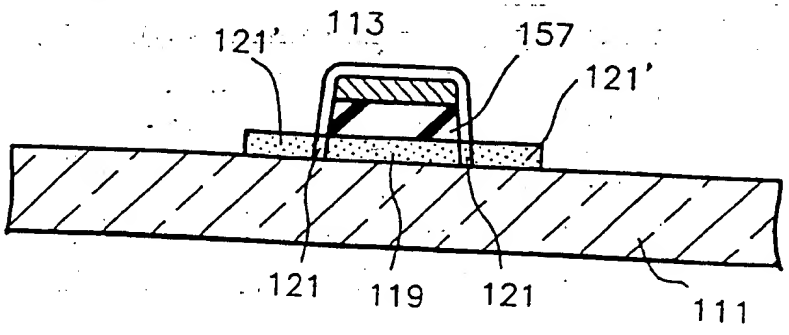


FIG. 13E

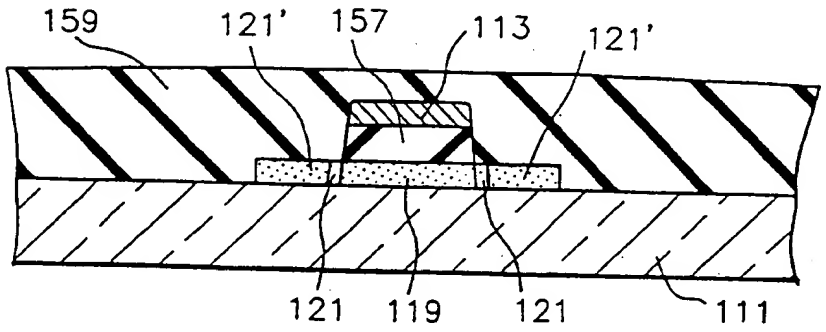


FIG. 13F

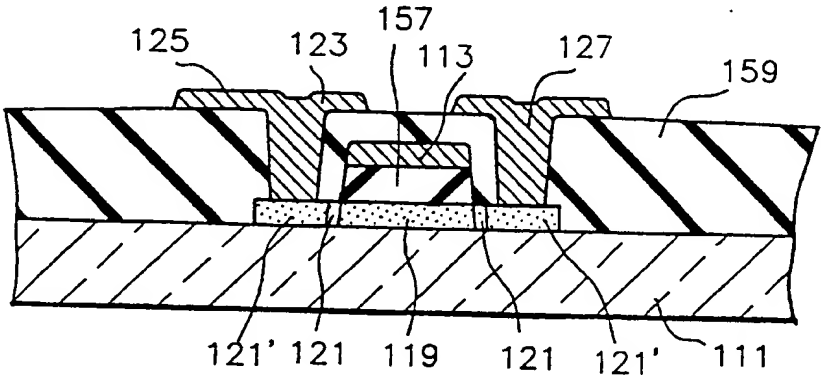


FIG. 13G

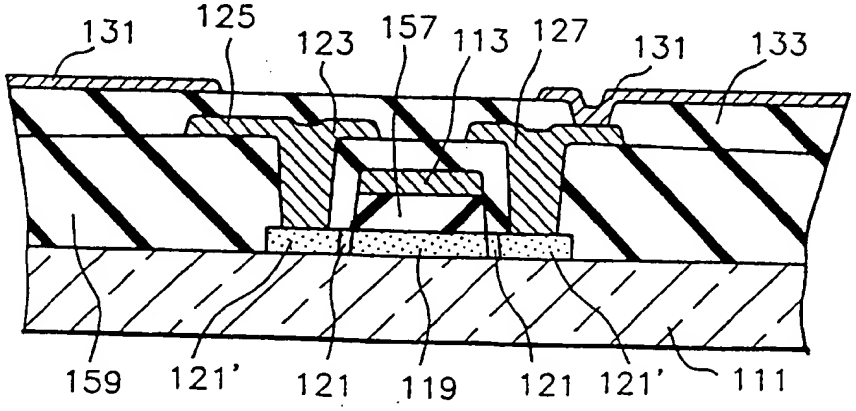


FIG. 14A

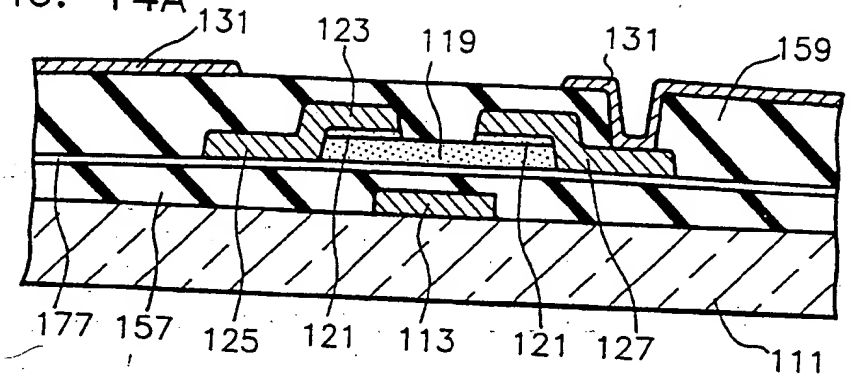


FIG. 14B

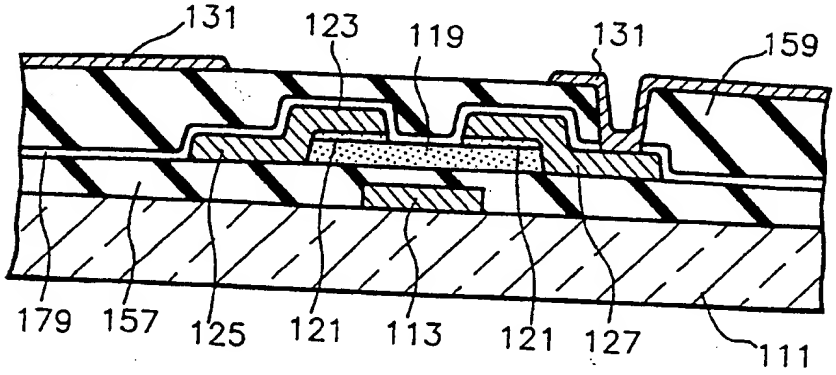


FIG. 14C

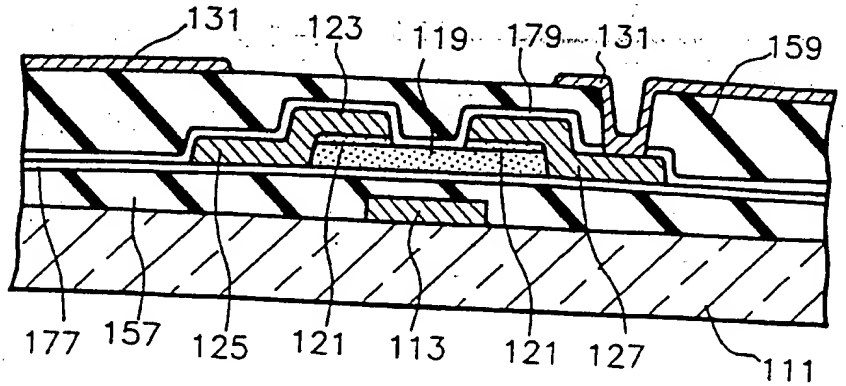


FIG. 14D

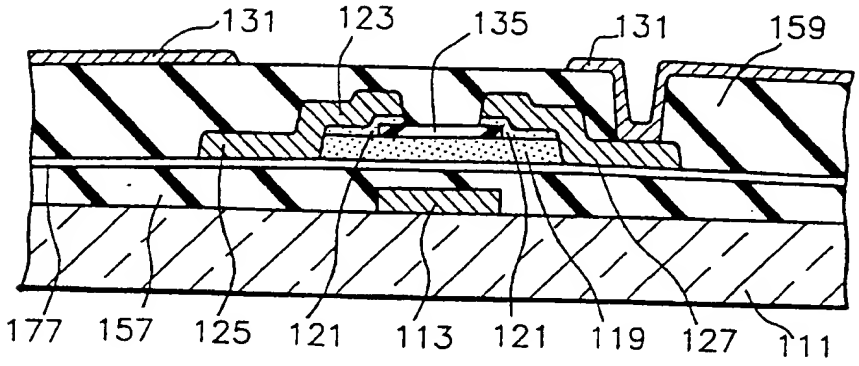


FIG. 14E

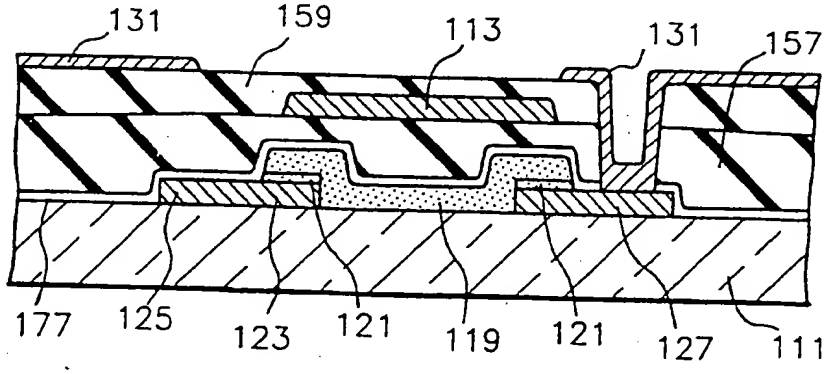


FIG. 14F

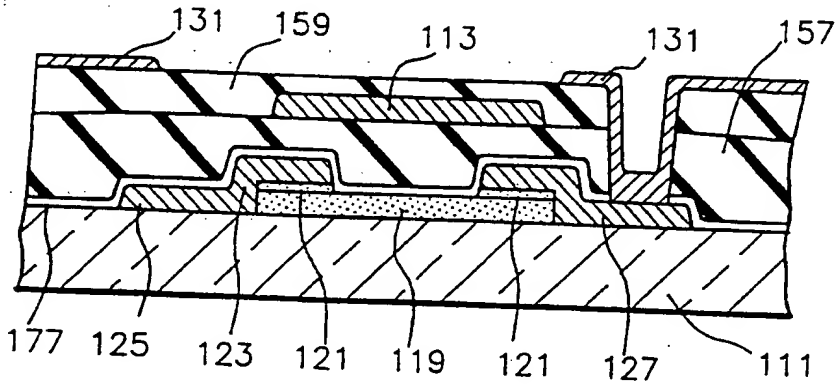


FIG. 14G

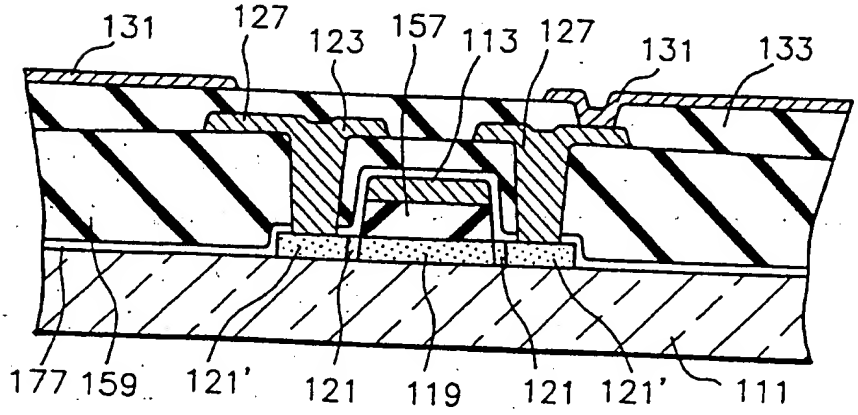


FIG. 15A

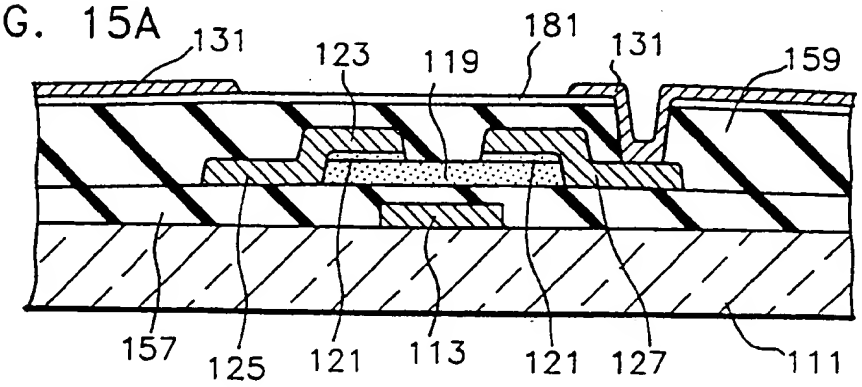


FIG. 15B

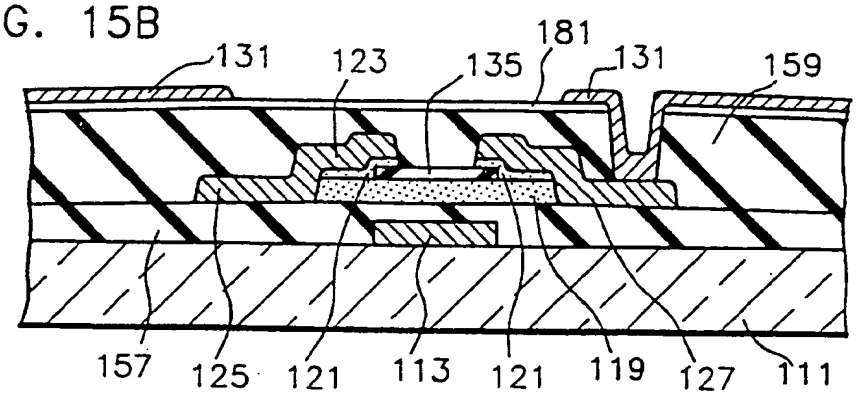


FIG. 15C

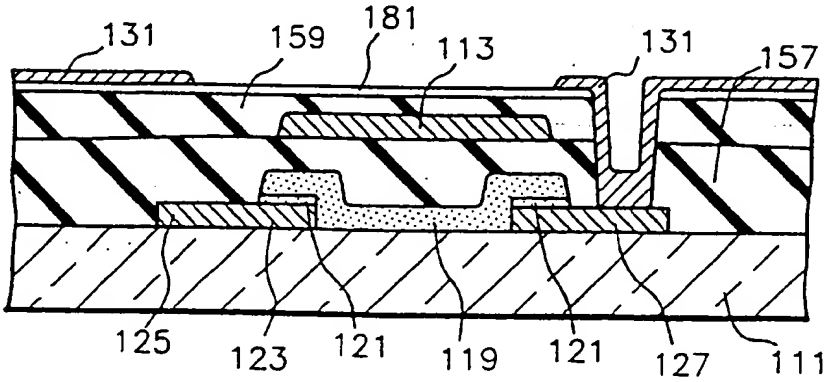


FIG. 15D

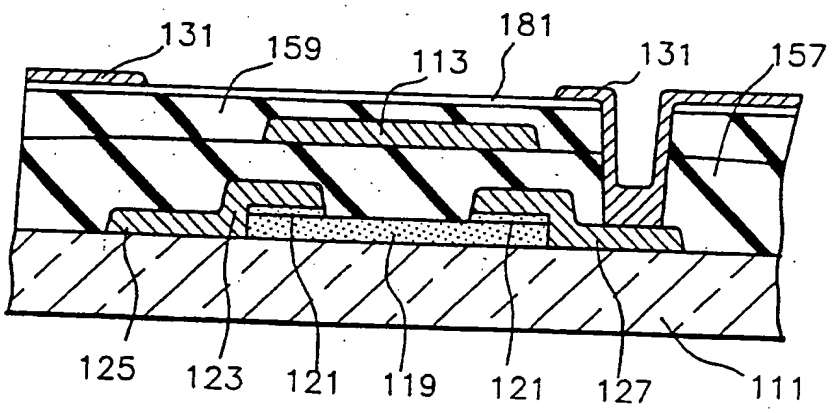


FIG. 15E

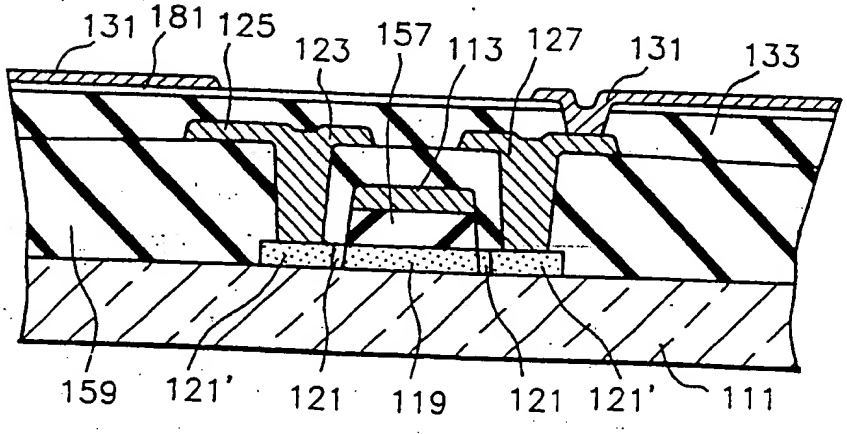


FIG. 16A

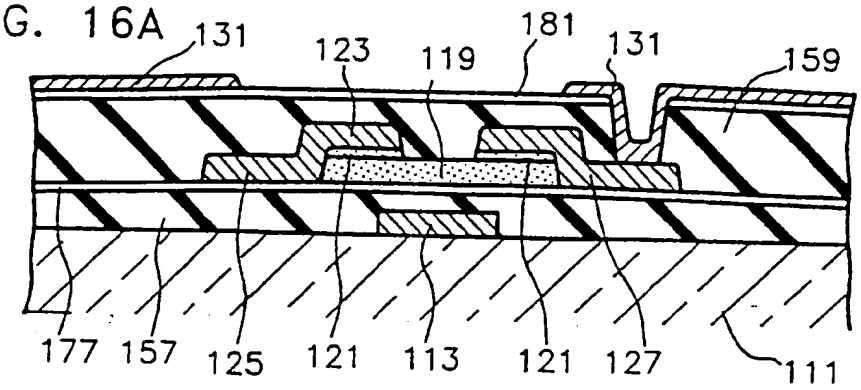


FIG. 16B

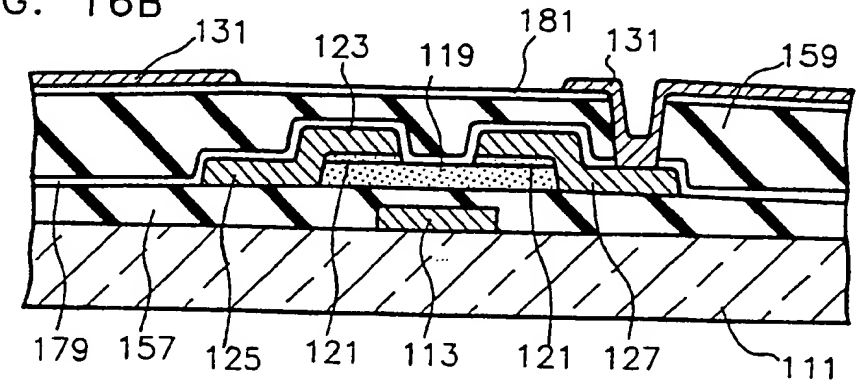


FIG. 16C

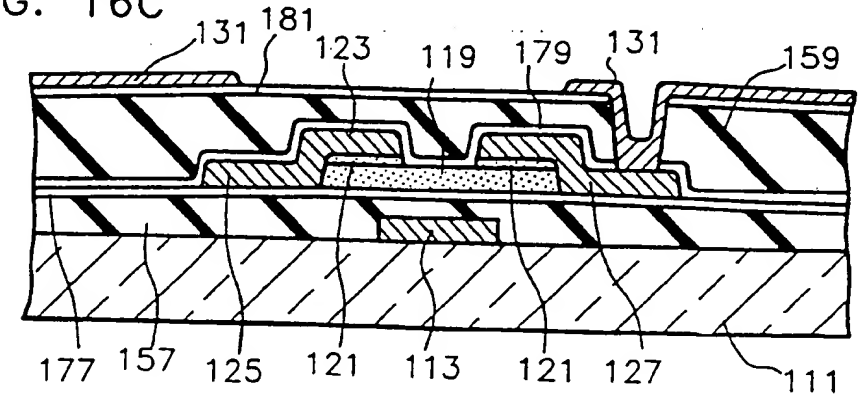


FIG. 16D

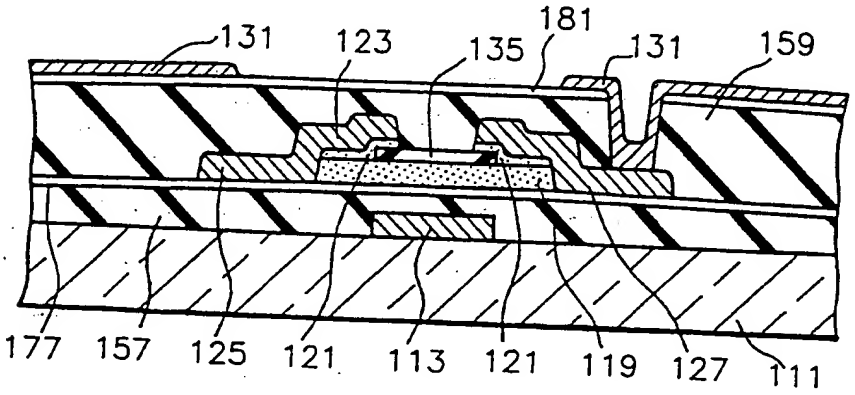


FIG. 16E

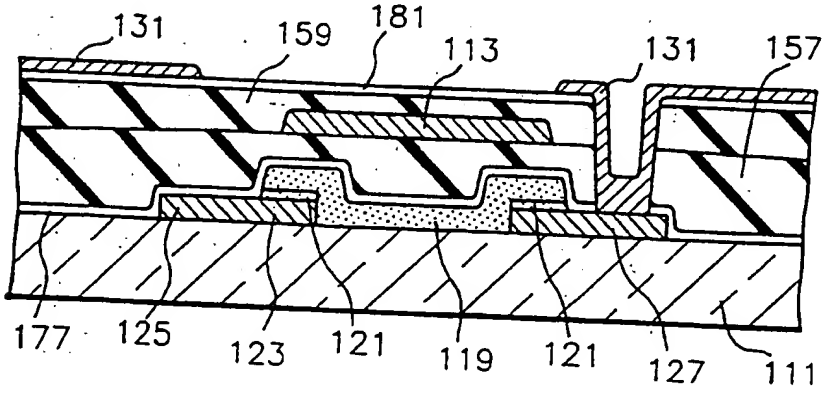


FIG. 16F

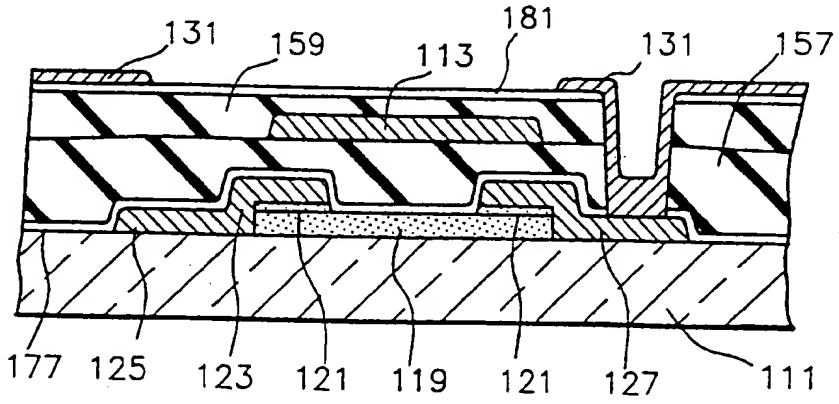


FIG. 16G

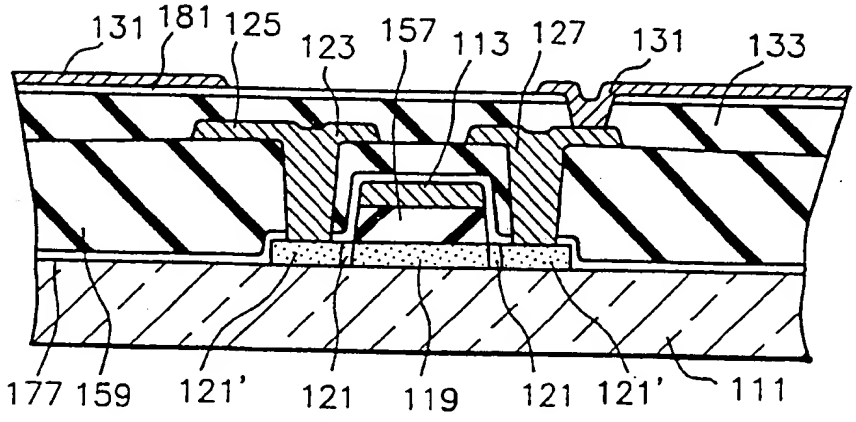


FIG. 17A

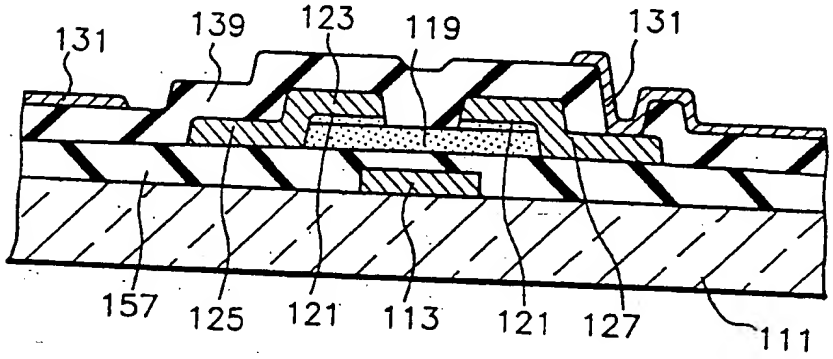


FIG. 17B

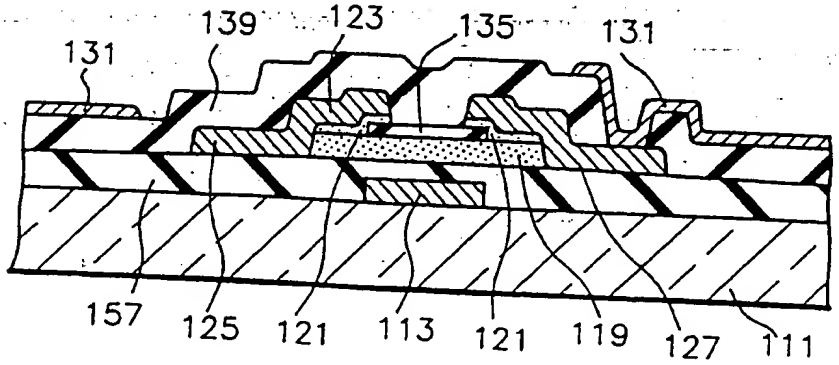


FIG. 17C

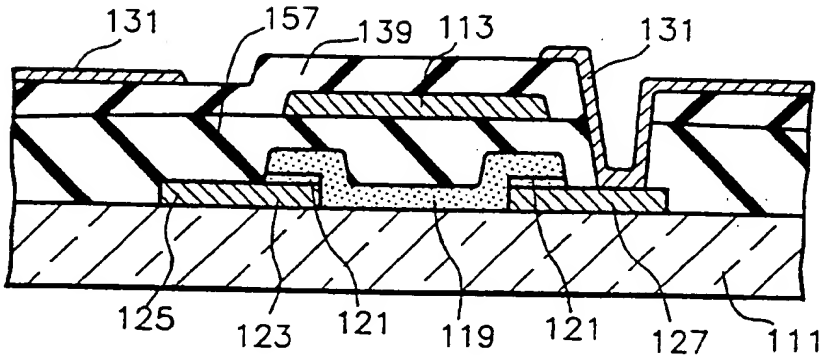


FIG. 17D

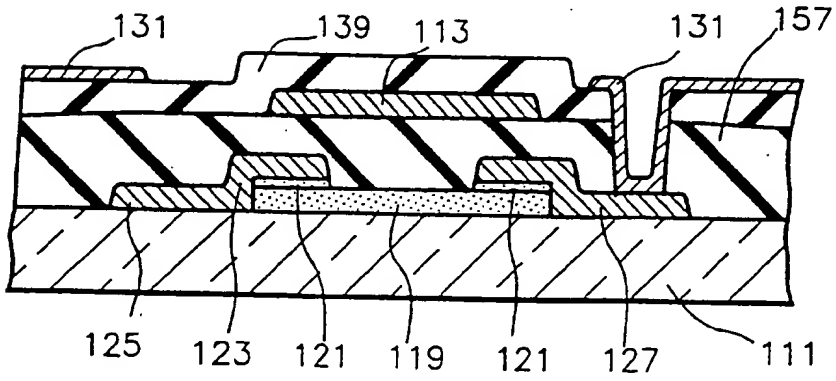


FIG. 18A

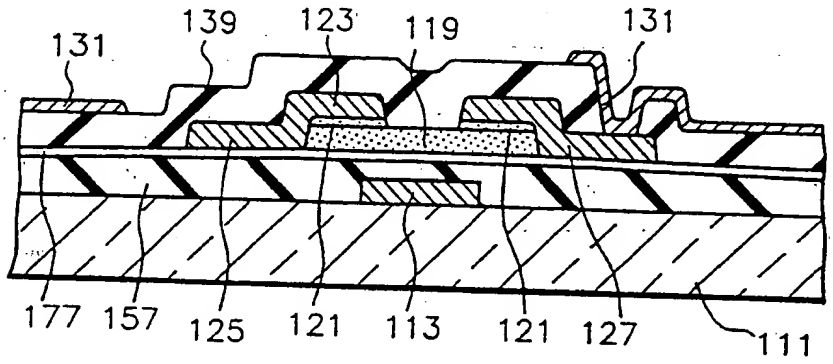


FIG. 18B

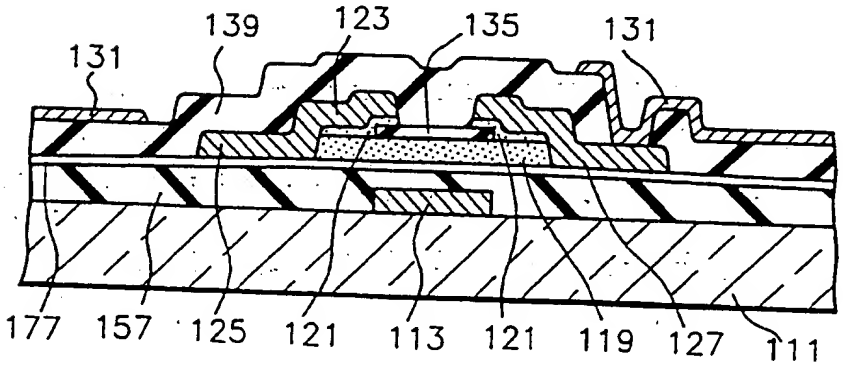


FIG. 18C

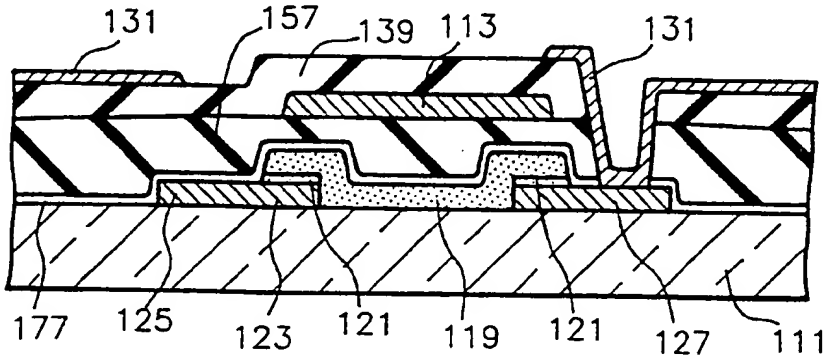


FIG. 18D

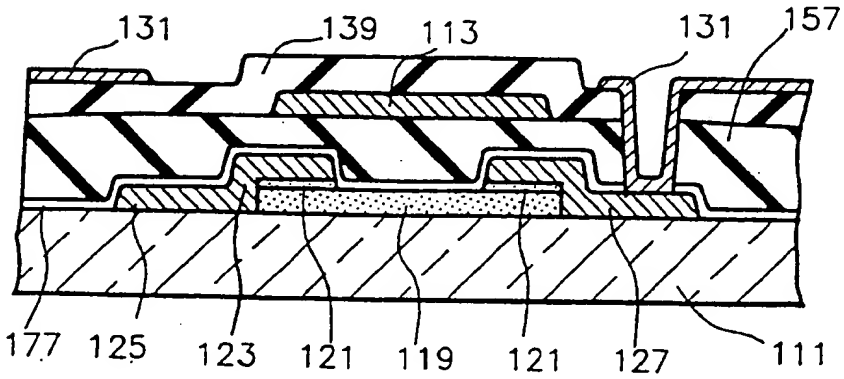


FIG. 19A

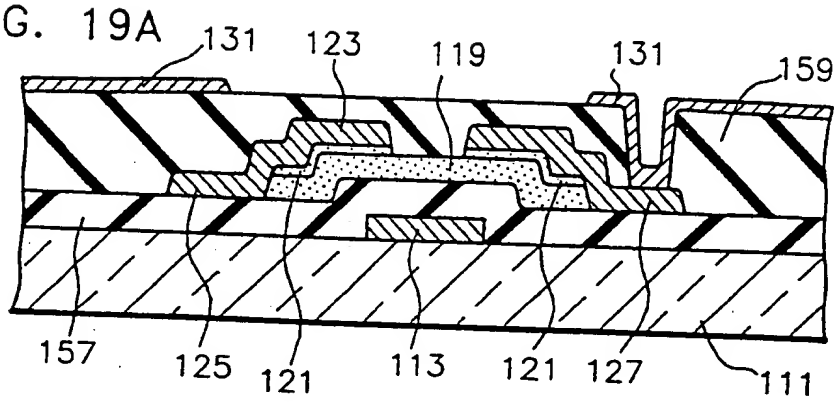


FIG. 19B

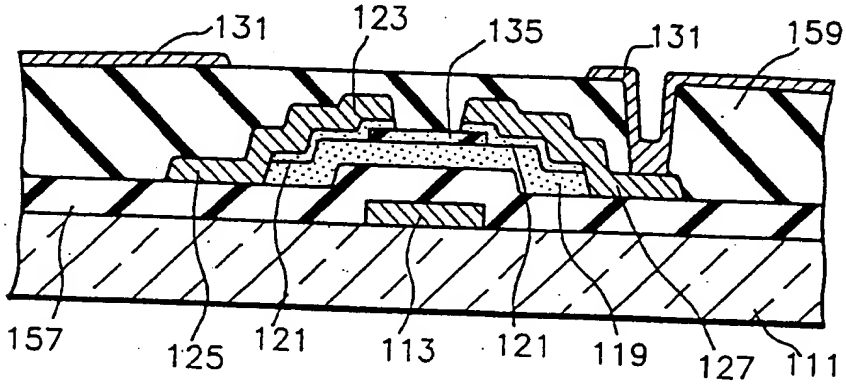


FIG. 19C

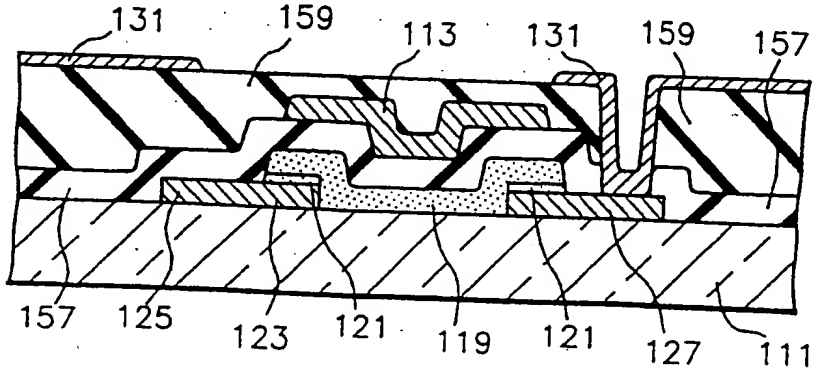


FIG. 19D

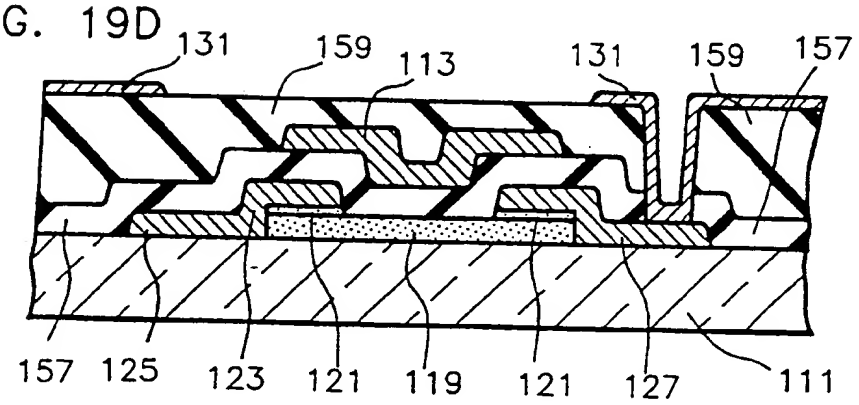


FIG. 19E

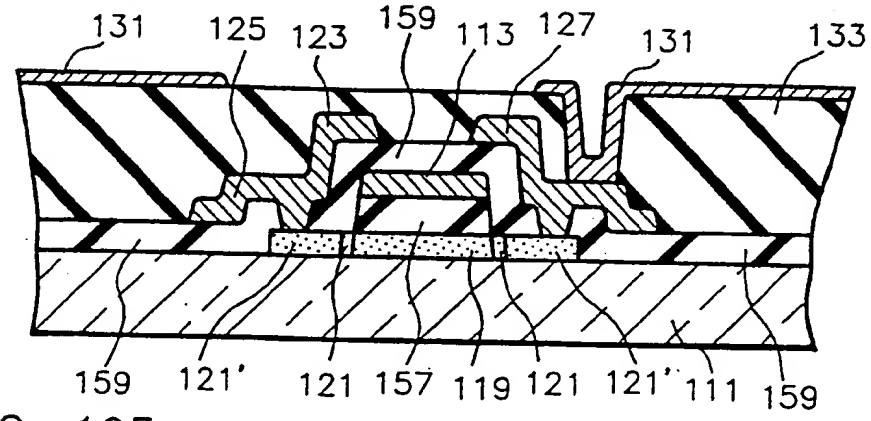


FIG. 19F

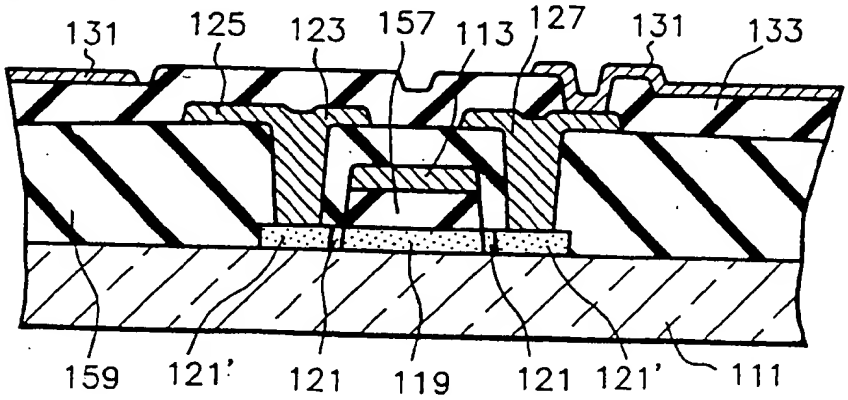


FIG. 20A

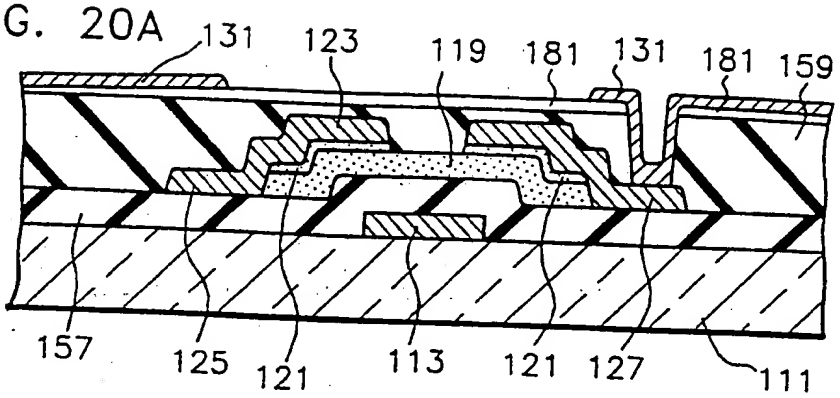


FIG. 20B

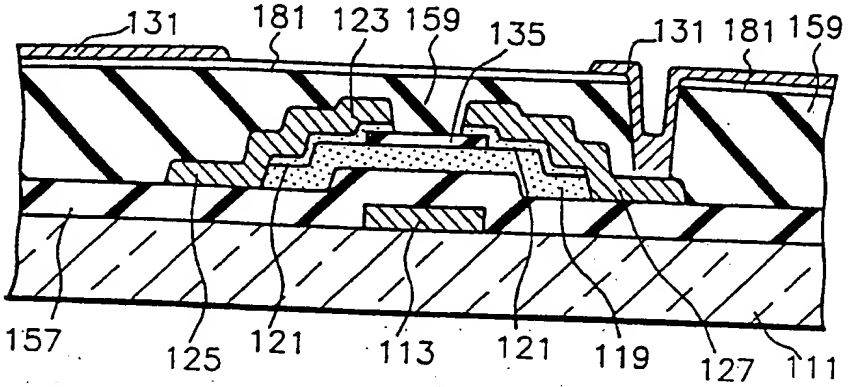


FIG. 20C

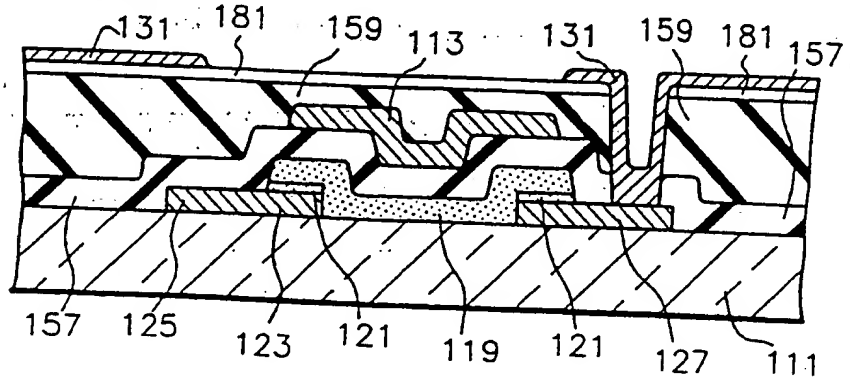


FIG. 20D

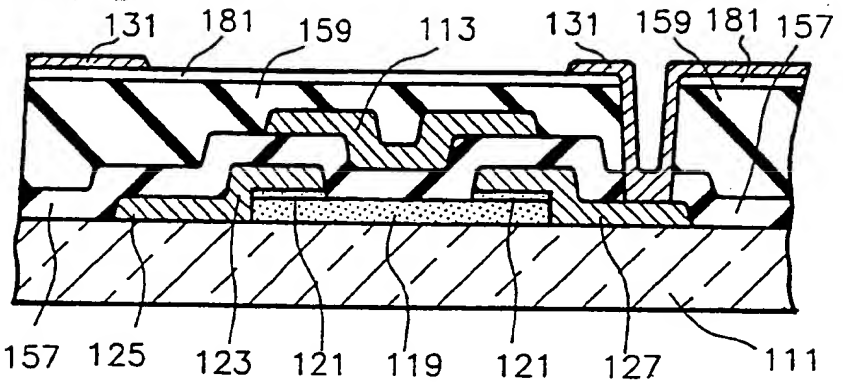


FIG. 20E

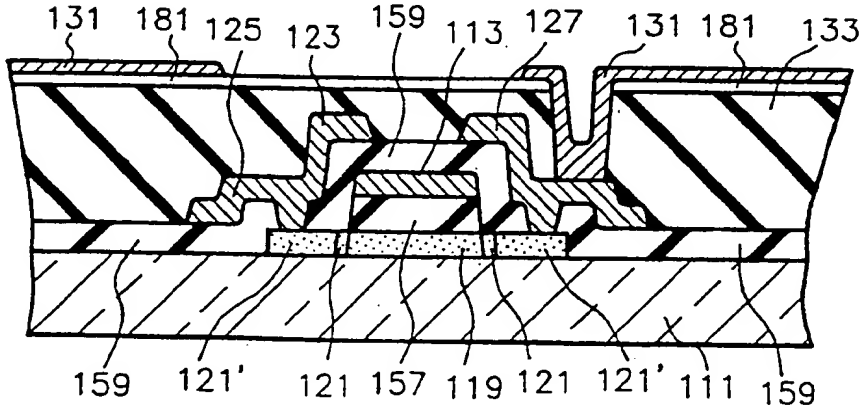


FIG. 21A

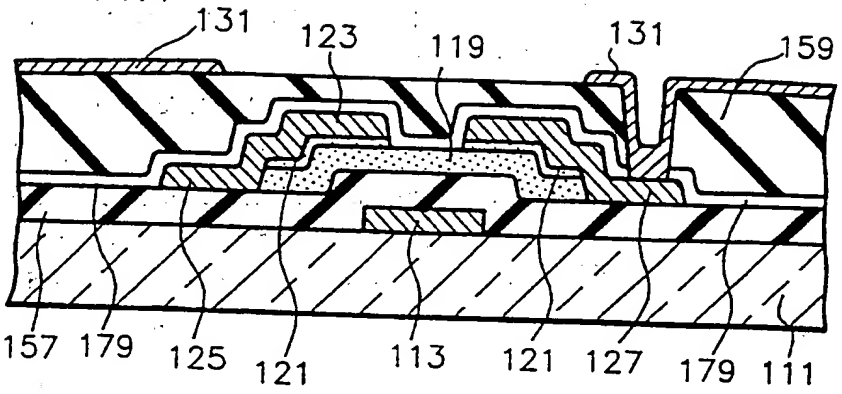
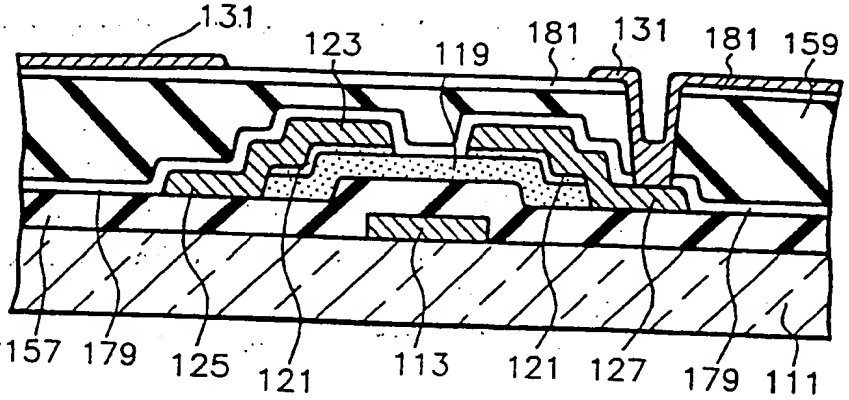


FIG. 21B



LIQUID CRYSTAL DISPLAY AND METHOD FOR MANUFACTURING THE SAME

The present invention relates to a liquid crystal display (LCD) and a method for manufacturing the same, and more particularly, but not exclusively, to a liquid crystal display having a thin film transistor and a method for manufacturing the same.

Recently, among various display devices for displaying picture information, a flat panel display device has been developed due to its advantages of light weight and portability. Among others, the development of an LCD is one of the most active research areas. This is because an LCD can provide a high quality image, a high resolution, and a high response speed necessary to display motion pictures.

The principle of an LCD resides in optical polarity and anisotropy of a liquid crystal. Transmission of a light is controlled by giving an optical anisotropy to liquid crystal molecules; aligning the liquid crystal molecules in different orientations using the polar nature of the liquid crystal molecules. An LCD is composed of two transparent substrates separated by a certain distance. A liquid crystal material is injected into the space between the substrates on which various elements are formed to drive the liquid crystal. In general, thin film elements such as thin film transistors are manufactured on one of the substrates (thin film transistor substrate). Therefore, the performance of an LCD depends significantly upon the method of manufacture and the structure of such thin film elements. Moreover, an active matrix liquid crystal display (AMLCD), which has recently been commercialized, shows various performance fluctuations depending on the method of manufacture, and the structure of the thin film transistor and other related elements. The details of a conventional active matrix liquid crystal display will be described below.

First, referring to FIG. 1, the structure of a conventional AMLCD is

reviewed. Rectangular pixels, each of which represents a point of picture information, are disposed to form a matrix array. Gate bus lines 15 and signal bus lines 25 are arranged in columns and rows defining the array. At the intersection between the gate bus line and the signal bus line, a switching element is formed. In general, a thin film transistor (TFT) is used as the switching element. The source electrode 23 of the TFT is connected to the signal bus line 25 (source bus line or data bus line) and the gate electrode 13 of the TFT is connected to the gate bus line 15. A pixel electrode 31 and a common electrode are formed at each pixel to apply an electric field to the liquid crystal. The pixel electrode 31 is connected to the drain electrode 27 of the TFT. Therefore, when the TFT is turned on by applying appropriate voltages to the gate and signal bus lines, the signal voltage is applied to the pixel electrode 31. This voltage creates an electric field between the pixel electrode and the common electrode. Then, the electric field forces the liquid crystal molecules to align in a certain orientation which depends on the field direction. Therefore, transmission of a light can be controlled by an artificial control of the orientation of the liquid crystal molecules. This characteristic of a liquid crystal is utilized to display picture information.

Second, a method for manufacturing a conventional AMLCD is reviewed. Two transparent substrates are prepared to construct an LCD. In general, the substrates are made of non- alkaline or soda glass. Different processes are applied to the two substrates. On the first substrate (upper plate), a color filter layer, a black matrix, common electrodes and bus lines are formed. On the second substrate (lower plate), switching elements such as TFTs, pixel electrodes and bus lines are formed.

This invention particularly relates to a second substrate of an AMLCD, on which TFTs are formed. Therefore, conventional methods for manufacturing the second substrate will be mainly described below.

There are various AMLCDs depending on the method of manufacture and

the structure. The AMLCDs can be classified according to the structure of a TFT. Typical structures of TFTs for an LCD are illustrated in FIGs. 2A to 5G.

FIGs. 2A to 2F taken along the line I-I in FIG.1, show an inverse staggered TFT, which uses amorphous silicon (a-Si) as a semiconductor layer. The method for manufacturing the inverse staggered TFT is as follows. A first metal, such as Ti, Cr, Ta, Al, Ti-Mo, Mo-Ta, or Al-Ta, (1000 to 2000 Å thick) is deposited on a glass substrate 11. The metal is patterned to form a gate bus line 15 and a gate electrode 13(FIG. 2A), followed by the overall deposition of silicon-nitride (SiN_x) to form a gate insulation layer 17 (FIG. 2B). A thin film of an amorphous semiconductor material such as a-Si and a thin film of an impurity-doped amorphous semiconductor material such as n^+ a-Si are sequentially deposited (1500 to 2000 Å thick and 300 to 500 Å thick, respectively) on the gate insulation film 17. They are patterned to form a semiconductor layer 19 and an impurity-doped semiconductor layer 21, as shown in FIG. 2B. Then, a second metal such a Cr, Mo, Ti, or Cr-Al (1000 to 2000 Å thick) is deposited and patterned to form a signal bus line 25, a source electrode 23, and a drain electrode 27. The exposed portion of the impurity-doped semiconductor layer 21 is removed using the source and drain electrodes as a mask. At this moment, the impurity-doped semiconductor layer 21 makes an ohmic contact with the source electrode 23 and the drain electrode 27 (FIG. 2C). Next, silicon nitride (SiN_x) is deposited to form a protection film 29 protecting the TFT formed under the film and providing an electrical insulation of the TFT from liquid crystal. Then, a contact hole is formed in the protection film 29 over the drain electrode 27, for connecting the drain electrode 27 to a pixel electrode, as shown in FIG. 2D. Indium tin oxide (ITO) 500 to 1000 Å thick, conducting metal, is deposited and patterned to form a pixel electrode 31, as shown in FIG. 2E. This completes the manufacture of the inverse staggered TFT.

Here, when removing the impurity-doped semiconducting layer 21 located between a source electrode and a drain electrode, a silicon nitride layer may be formed as an etch stopper 35 to prevent the over-etching of the semiconducting layer 19, as shown in FIG. 2F.

FIGs. 3A to 3D show a staggered TFT, which uses an amorphous silicon (a-Si) as the semiconductor layer. The structure is inverse to the inverse staggered TFT described above. The method for manufacturing a staggered TFT structure is as follows. A first metal and an impurity-doped semiconductor material are deposited on a glass substrate 11. They are patterned to form a signal bus line 25, a source electrode 23, a drain electrode 27, and an impurity-doped semiconductor layer 21, as shown in FIG. 3A. Then, an amorphous silicon material, an insulation material such as SiN_x or SiO_2, and a second metal are sequentially deposited on the whole substrate including the impurity-doped semiconductor layer, and patterned at once to form a semiconductor layer 19, a gate insulation layer 17, a gate bus line (not shown in the drawings) and a gate electrode 13, respectively. The exposed portion of the impurity-doped semiconductor layer 21 is then removed, as shown in FIG. 3B. Here, the impurity-doped semiconductor layer 21 makes an ohmic contact with the source electrode 23 and the drain electrode 27. Next, a protection layer 29 is formed on the overall surface (FIG. 3C). A contact hole is formed in the protection layer 29 above the drain electrode 27. Finally, a pixel electrode 31 is formed and connected to the drain electrode 27 through the contact hole (FIG. 3D). This completes the manufacture of the staggered TFT.

FIGs. 4A to 4D show a coplanar TFT which uses polycrystalline silicon intrinsic semiconductor material (Poly-Si) as the semiconductor layer. The method for manufacturing a coplanar TFT is as follows. A polycrystalline semiconductor material such as poly-Si and an impurity-doped polycrystalline semiconductor material are sequentially deposited on a transparent glass substrate

11 and patterned to form a semiconductor layer 19 and an impurity-doped semiconductor layer 21, as shown in FIG. 4A. Then, a first metal such as Al or an Al alloy is deposited and patterned to form a signal bus line 25, a source electrode 23 and a drain electrode 27. The exposed portion of the impurity-doped semiconductor layer 21 located between the source and drain electrodes is removed subsequently (FIG. 4B). Here, the impurity-doped semiconductor layer 21 makes an ohmic contact with the source and drain electrodes. Next, silicon oxide (SiO_2) is deposited and patterned to form a gate insulation layer 17. Subsequently, a second metal such as Cr is deposited and patterned to form a gate bus line and a gate electrode 13. Then, silicon oxide (SiO_2) is deposited to form a protection film 29, as shown in FIG. 4C. A contact hole is formed in the protection film 29 on the drain electrode 27. Finally, a pixel electrode 31 is formed by the deposition and patterning of ITO, and connected to the drain electrode 27 through the contact hole (FIG. 4D). This completes the manufacture of the coplanar TFT.

FIGs. 5A to 5G show a self-aligned coplanar TFT. The method for manufacturing a self-aligned coplanar TFT is as follows. A semiconductor layer 19 is formed on a transparent substrate 11 by depositing and patterning a polycrystalline intrinsic semiconductor material. There are three methods to form a polycrystalline semiconductor layer, in general. First, polycrystalline silicon is formed by depositing an amorphous silicon and annealing it by laser. Second, polycrystalline silicon is formed by depositing an amorphous silicon and thermally annealing it. Third, a polycrystalline silicon material is directly deposited. After forming the semiconductor layer 19, silicon oxide and a first metal are sequentially deposited and patterned to form a gate insulation layer 17, a gate electrode 13, and a gate bus line (not shown in the drawings) as shown in FIG. 5B. At this time, the gate electrode 13 and the gate insulation layer 17 should be formed substantially at the center of the semiconductor layer 19. As

shown in Fig. 5C, the edge portion of the semiconductor layer 19 are turned into a first impurity-doped semiconductor layers 21 by injecting impurity-ions into the semiconductor layer 19 using the gate electrode 13 as a mask (dopant concentration 10^{14} to 10^{15} cm^{-3}). Then, a photoresist is coated to cover a desired portion of the first impurity-doped semiconductor layer 21. Subsequently, as shown in FIG. 5D, a second impurity-doped semiconductor layer 21' is formed by injecting impurity-ions (dopant concentration 10^{16} to 10^{18} cm^{-3}). The first impurity-doped semiconductor layer 21 is a lightly-doped drain (LDD) part with impurity ions having lower density than the second impurity-doped semiconductor layer 21'.

Here, the impurity injecting step described by referring to FIG. 5C can be omitted. In this case, a photoresist is coated to cover a certain part of the semiconductor layer 19, an impurity-doped semiconductor layer 21' is formed by injecting impurity-ions (dopant concentration 10^{16} to 10^{18} cm^{-3}). The part covered by the photoresist becomes an offset part with no injected ions.

Next, a first protection film 29 is formed by depositing silicon oxide on the whole surface, as shown in FIG. 5E. First contact holes are formed in the protection film 29. A second metal is deposited and patterned to form a signal bus line 25, a source electrode 23, and a drain electrode 27, which are connected to the impurity-doped semiconductor layer 21' through the contact holes. Then, ITO is deposited and patterned to form a pixel electrode 31 connected to the drain electrode 27, as shown in FIG. 5F. Alternatively, a second protection film 33 covering the source and drain electrodes may be deposited on the whole surface after depositing and patterning the second metal, and then a second contact hole and the pixel electrode may be formed (FIG. 5G).

The above-described conventional AMLCDs have the following drawbacks. First, as shown in FIG. 6, a stepped surface appears due to a multilayer structure of the TFT and bus lines. The figure shows the structure in

which the gate insulation layer 17 is deposited on the gate bus line 15, and the signal bus line 25 is formed so as to cross the gate bus line. Thus, line disconnection and short circuit may occur at the intersection between the signal bus line and the gate bus line. Second, high parasitic capacitance is generated when a pixel electrode overlaps one of the bus lines, because an inorganic film such as SiN_x or SiO_x has a relatively high dielectric constant. Therefore, a pixel electrode is formed so as to have a predetermined space between the pixel electrode and the bus lines, as shown in FIG. 1. In this case, since the back-scattered light passing through the space is undesirable, a black matrix, which blocks the back-scattered light, is formed to cover the space between the bus line and the pixel electrode. This structure, however, has an insufficient aperture ratio. Third, after coating an alignment film for liquid crystal, a rubbing process is necessary for setting a pre-tilting angle in the alignment film, which determines the initial orientation of liquid crystal. The rubbing process, however, does not work properly on a surface with significant steps, and a domain phenomenon occurs and yields a different orientation condition from the intended one, which reduces the quality of the LCD.

The best or at least a good solution to these problems is to smooth the stepped profile due to the multilayer structure. Using a material having a high planarization property for a gate insulation layer and/or a protection film achieves this purpose. Examples of such material having the high planarization property have been introduced in Japanese patents: 4-163528, 83-289965, 4-68318, and 63-279228.

These patents use polyimide or acryl resin as a protection film in order to obtain a smooth surface over the TFT. However, since the adhesion property between the resins and ITO (a pixel electrode) is poor, it is necessary to form a thin intermediate layer of an inorganic material prior to the ITO deposition to prevent the detachment of ITO during the patterning. In addition, the upper

processing temperature for these materials, ranging from 350 to 400 °C, is too high for a protection film of a TFT. In general, when the processing temperature for the insulation or protection film is higher than 250 °C, the TFT characteristics may be affected by temperature. Also, the dielectric constant of polyimide is 3.4 to 3.8, similar to that of SiN_x, 3.5. Therefore, a parasitic capacitance can not be sufficiently reduced.

It is evident that the problem associated with the stepped surface can be solved by the use of a material that has a smooth surface when applied for a protection or insulation layer. However, it is difficult to select such a material, taking into account various conditions/environment of an LCD. The following conditions should be met for a material used as an insulation or protection film.

First, the material should have a low dielectric constant when used for electrical insulation such as gate insulation, to prevent errors in the TFT operation by parasitic capacitance. The dielectric constants of SiN_x and SiO_2 for a conventional use are about 7 and 4, respectively. Second, the material should have a superior insulation property: high intrinsic resistivity. Third, when used as a protection film, the material should have a good adhesion property to ITO which is deposited on the protection film to form a pixel electrode.

Accordingly, the present invention is directed to a liquid crystal display and a method for manufacturing the same that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an LCD whose surface does not have stepped profile due to a multilayered structure.

Another object of the present invention is to provide an LCD which has less parasitic capacitance.

Another object of the present invention is to provide an LCD which is free from problems such as electron trap and poor adhesion at the interface between an insulation layer and a semiconductor layer.

A further object of the present invention is to provide an LCD which has

an improved aperture ratio.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the liquid crystal display includes a substrate; a thin film transistor over the substrate, the thin film transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulating layer; and a protection film over the thin film transistor, wherein the protection film includes a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB(perfluorocyclobutane), or BCB(benzocyclobutene).

The protection film may include at least one of fluorinated polyimide teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB(perfluorocyclobutane), or BCB(benzocyclobutene).

In another aspect, the liquid crystal display includes a substrate; and a thin film transistor over the substrate, the thin film transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulating layer, wherein the gate insulating layer includes a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB.

In another aspect, the method for manufacturing an LCD which has switching elements including signal electrodes, insulating layers, semiconductor layers, impure semiconductor layers, data electrodes and out-put electrodes, data bus lines connected with the data electrodes, protection layers protecting the switching elements, and pixel electrodes, all of them being formed on a

substrate, includes the steps of forming at least one of the insulating layer and the protection layer with an organic material.

In another aspect, the method for manufacturing an LCD includes the steps of depositing a first metal on a substrate and forming a gate bus line and a gate electrode by patterning the first metal; forming a gate insulating layer by depositing organic material on the whole surface of the substrate on which the gate bus line and the gate electrode are already formed; sequentially depositing intrinsic semiconductive material and impure semiconductive material on the gate insulating layer and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a second metal on the whole surface of the substrate on which the impure semiconductor layer is already formed and forming a source bus line, a source electrode and a drain electrode by patterning the second metal layer; forming a protection layer by depositing inorganic material on the whole surface of the substrate on which the source and drain electrodes are formed; forming a contact hole in a portion of the protection layer over the drain electrode; and depositing a transparent conductive material on the whole surface of the substrate on which the protection layer with inorganic material is formed subsequently and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing a first metal and an impure semiconductive material on a substrate and forming a source bus line, a source electrode, a drain electrode and an impure semiconductive material; depositing intrinsic semiconductor material on the substrate on which the impure semiconductor layer is formed and forming a semiconductor layer patterning the intrinsic semiconductive material; forming a gate insulating layer by depositing an organic

material on the whole surface of the substrate on which the semiconductor layer is formed; depositing a second metal on the gate insulating layer and forming a gate electrode and a gate bus line by patterning the second metal; forming a protection layer by depositing an inorganic material on the whole surface of the substrate on which the gate electrode and the gate bus line are formed; forming a contact hole in a portion of the gate insulating layer and the protection layer over the drain electrode; and depositing a transparent conductive material on the protection layer and forming a pixel electrode by patterning the transparent conductive material layer.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing an intrinsic semiconductive material and an impure semiconductive material on a substrate and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a first metal on the substrate on which the impure semiconductor layer is formed and forming a source bus line, a source electrode and a drain electrode by patterning the first metal; forming a gate insulating layer by depositing organic material on the whole surface of the substrate on which the source and drain electrodes are formed; depositing a second metal on the gate insulating layer and forming a gate bus line and a gate electrode by patterning the second metal; forming a protection layer by depositing inorganic material on the whole surface of the substrate on which the gate electrode is formed; forming a contact hole in the insulating layer and the protection layer over the drain electrode; and depositing a transparent conductive material on the protection layer and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the method for manufacturing an LCD includes the

steps of depositing a first metal on a substrate and forming a gate bus line and a gate electrode by patterning the first metal; forming a gate insulating layer by depositing an inorganic material on the whole surface of the substrate on which the gate bus line and the gate electrode are formed; sequentially depositing an intrinsic semiconductive material and an impure semiconductive material on the gate insulating layer and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a second metal on the whole surface of the substrate on which the impure semiconductor layer is formed and forming a source bus line, a source electrode and a drain electrode by patterning the second metal; forming a protection layer by depositing organic material on the whole surface of the substrate on which the source and drain electrodes are formed; forming a contact hole in a portion of the protection layer covering the drain electrode; and depositing a transparent conductive material on the substrate on which the protection layer is formed and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing a first metal and an impure semiconductive material on a substrate and forming a source bus line, a source electrode, a drain electrode and an impure semiconductor layer by patterning the first metal and the impure semiconductive material; depositing intrinsic semiconductor material on the substrate on which the semiconductor layer is formed and forming a semiconductor layer by patterning the intrinsic semiconductive material; forming a gate insulating layer by depositing inorganic material on the whole surface of the substrate on which the semiconductor layer is formed; depositing a second metal on the gate insulating layer and forming a gate electrode and a gate bus line by patterning the second metal; forming a protection layer by depositing organic material on the whole

surface of the substrate on which the gate electrode and the gate bus line are formed; forming a contact hole in the gate insulating layer and the protection layer over the drain electrode; and depositing a transparent conductive material on the passivation layer and forming a pixel electrode by patterning the transparent conductive material.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing an intrinsic semiconductive material and an impure semiconductive material on a substrate and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a first metal on the substrate on which the impure semiconductor layer is formed and forming a source bus line, a source electrode and a drain electrode by patterning the first metal; forming a gate insulating layer by depositing inorganic material on the whole surface of the substrate on which the source and drain electrodes are formed; depositing a second metal on the gate insulating layer and forming a gate bus line and a gate electrode by patterning the second metal; forming a protection layer by depositing organic material on the whole surface of the substrate on which the gate electrode is formed; forming a contact hole in the insulating layer and the protection layer over the drain electrode; and depositing a transparent conductive material on the protection layer and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the method for manufacturing an LCD includes the steps of depositing a first metal on a substrate and forming a gate bus line and a gate electrode by patterning the first metal; forming a gate insulating layer by depositing an organic material on the whole surface of the substrate on which the gate bus line and the gate electrode are formed; sequentially depositing an intrinsic semiconductive material and an impure semiconductive material on the

gate insulating layer and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a second metal on the whole surface of the substrate on which the impure semiconductor layer is formed and forming a source bus line, a source electrode and a drain electrode by patterning the second metal; forming a protection layer by depositing an organic material on the whole surface of the substrate on which the source and drain electrodes are formed; forming a contact hole in a portion of the protection layer covering the drain electrode; and depositing a transparent conductive material on whole surface of the substrate on which the protection is formed and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing a first metal and an impure semiconductive material on a substrate and forming a source bus line, a source electrode, a drain electrode and an impure semiconductor layer by patterning the first metal and the impure semiconductive material; depositing an intrinsic semiconductive material on the substrate on which the impure semiconductor layer is formed and forming a semiconductor layer by patterning the intrinsic semiconductive material; forming a gate insulating layer by depositing an organic material on the whole surface of the substrate on which the semiconductor layer is formed; depositing a second metal on the gate insulating layer and forming a gate electrode and a gate bus line by patterning the second metal; forming a protection layer by depositing organic material on the whole surface of the substrate on which the gate electrode and the gate bus line are formed; forming a contact hole in the gate insulating layer and the protection layer over the drain electrode; and depositing a transparent conductive material on the protection layer and forming a pixel electrode by patterning transparent conductive material.

In another aspect, the method for manufacturing an LCD includes the steps of sequentially depositing an intrinsic semiconductive material and an impure semiconductive material on a substrate and forming a semiconductor layer and an impure semiconductor layer by patterning the intrinsic semiconductive material and the impure semiconductive material; depositing a first metal on the substrate on which the impure semiconductor layer is formed and forming a source bus line, a source electrode and a drain electrode by patterning the first metal; forming a gate insulating layer by depositing an organic material on the whole surface of the substrate on which the source and drain electrodes are formed; depositing a second metal on the gate insulating layer and forming a gate bus line and a gate electrode by patterning the second metal; forming a protection layer by depositing an organic material on the whole surface of the substrate on which the gate electrode is formed; forming a contact hole in the insulating layer and the protection layer covering the drain electrode; and depositing a transparent conductive material on the whole surface of the protection layer and forming a pixel electrode by patterning the transparent conductive material, the pixel electrode being electrically connected with the drain electrode through the contact hole.

In another aspect, the LCD showing picture information includes a substrate, signal bus lines and data bus lines formed on the substrate, switching elements being connected with the signal and data lines, a protection layer, made of insulating material and protecting the switching elements, and pixel electrodes driven by the switching elements, in which at least one of the components of the switching elements and the protection layer is made of organic material.

In another aspect, the LCD showing picture information includes a substrate; gate bus lines delivering signals of the picture information; gate electrodes which are branched out from the gate bus lines; a gate insulating layer, made of organic material, covering the gate bus lines and the gate electrodes; a semiconductor layer formed on the

gate insulating layer; an impure semiconductor layer formed on the semiconductor layer; source bus lines delivering the picture information; source electrodes which are branched out from the source bus lines and connected with the semiconductor layer; drain electrodes which are opposite to the source electrodes and connected with the semiconductor layer; a protection layer covering the above mentioned elements formed on the substrate; and pixel electrodes being electrically connected with the drain electrodes.

In another aspect, the LCD showing picture information includes a substrate; gate bus lines delivering signals of the picture information; gate electrodes which are branched out from the gate bus lines; a gate insulating layer covering the gate bus lines and the gate electrodes; a semiconductor layer formed on the gate insulating layer; an impure semiconductor layer formed on the semiconductor layer; source bus lines delivering data of the picture information; source electrodes which are branched out from the source bus lines and connected with the semiconductor layer; drain electrodes which are opposite to the source electrodes and connected with the semiconductor layer; a protection layer, made of organic material, covering the above mentioned elements formed on the substratically connected with the drain electrodes.

In another aspect, the LCD showing picture information includes a substrate; gate bus lines delivering signals of the picture information; gate electrodes which are branched out from the gate bus lines; a gate insulating layer, made of an organic material, covering the gate bus lines and the gate electrodes; a semiconductor layer formed on the gate insulating layer; an impure semiconductor layer formed on the semiconductor layer; source bus lines delivering data of the picture information; source electrodes which are branched out from the source bus lines and connected with the semiconductor layer; drain electrodes which are opposite to the source electrodes and connected with the semiconductor layer; a protection layer, made of an organic material, covering the above mentioned elements; and

pixel electrodes being electrically connected with the drain electrodes.

In another aspect, a transistor substrate for a liquid crystal display includes a substrate; a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer; and a protection layer over the transistor, the protection layer including a material derived from fluorinated polyimide, teflon, cytop, fluoroppolyarylether, fluorinated para-xylene, PFCB or BCB.

In another aspect, a transistor substrate for a liquid crystal display includes a substrate; and a TFT over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer, the gate insulation layer including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

In another aspect, a method for manufacturing a TFT on a substrate for a liquid crystal display includes the steps of forming a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer; and forming a protection layer over the transistor, the protection layer including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

In a further aspect, a method for manufacturing a TFT on a substrate for a liquid crystal display includes the steps of forming a TFT over the substrate, the TFT having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer, wherein the gate insulation layer includes a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

For a better understanding of the invention, embodiments will now be

described by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a plan view of a conventional liquid crystal display;

FIGs. 2A to 2F are cross-sectional views of an inverse staggered type thin film transistor for a conventional liquid crystal display, taken along line I-I in FIG. 1;

FIGs. 3A to 3D are cross-sectional views of a staggered type thin film transistor for a conventional liquid crystal display, taken along line I-I in FIG. 1;

FIGs. 4A to 4D are cross-sectional views of a coplanar type thin film transistor for a conventional liquid crystal display, taken along line I-I in FIG. 1;

FIGs. 5A to 5G are cross-sectional views of a self-aligned coplanar type thin film transistor for a conventional liquid crystal display, taken along line I-I in FIG. 1;

FIG. 6 is a perspective view showing a multilayer structure of thin films for a conventional liquid crystal display;

FIGs. 7A and 7B show the I-V characteristics of the TFT in a liquid crystal display having an organic material;

FIG. 8 is a perspective view showing a multilayer structure of thin films for a liquid crystal display using an organic material according to the present invention;

FIG. 9 is a plan view of a liquid crystal display according to the present invention;

FIGs. 10A to 10G are cross-sectional views of a liquid crystal display using an inverse staggered type transistor according to a first embodiment of the present invention, taken along line II-II in FIG. 9;

FIGs. 11A to 11F are cross-sectional views of a liquid crystal display using a staggered type transistor according to a second embodiment of the present invention, taken along line II-II in FIG. 9;

FIGs. 12A to 12F are cross-sectional views of a liquid crystal display using a coplanar type transistor according to a third embodiment of the present invention, taken along line II-II in FIG. 9;

FIGs. 13A to 13G are cross-sectional views of a liquid crystal display using a self-aligned coplanar type transistor according to a fourth embodiment of the present invention, taken along line II-II in FIG. 9;

FIGs. 14A to 14G are cross-sectional views of various thin film transistors for a liquid crystal display according to a fifth embodiment of the present invention;

FIGs. 15A to 15E are corss-sectional views of various thin film transistor for a liquid crystal display using an inorganic layer between the protection layer made of the organic layer and pixel electrode according to a sixth embodiment of the present invention; and

FIGs. 16A to 16G are cross-sectional views of various thin film transistors for a liquid crystal display using a first inorganic layer between the protection layer made of the organic layer and pixel electrode, and a second inorganic layer between semiconductor and organic layers according to a sixth embodiment of the present invention; and

FIGs. 17A to 17D are cross-sectional views showing the structures of various thin film transistors according to a seventh embodiment of the present invention; and

FIGs. 18A to 18D are cross-sectional views showing the structures of various thin film transistors according to a seventh embodiment of the present invention, wherein an inorganic layer is formed beween semiconductor and gate insulation layer; and

FIGs. 19A to 19F are cross-sectional views showing the structures of various thin film transistors according to a eighth embodiment of the present invention; and

FIGs. 20A to 20E are cross-sectional views showing the structures of various thin film transistors according to a eighth embodiment of the present invention, wherein an inorganic layer is formed between pixel electrode and the protection layer; and

FIGs. 21A and 21B are cross-sectional views showing the structures of various thin film transistors, especially inverse staggered structure, according to a eighth embodiment of the present invention.

Before discussing the details of the preferred embodiments of the present

invention, information regarding organic materials is discussed.

This invention uses an organic material having a high planarization property, as it complies with the conditions mentioned above. However, new problems could arise when using an organic material for an insulation film and a protection film in an LCD. These are as follows.

A technology relating to the manufacture of a TFT is most important and complicated in the manufacture of an LCD which uses a thin film transistor as a switching element. In particular, the performance of the switching element depends upon the selection of TFT materials. When a new TFT material is tried, it is difficult to anticipate the resultant performance of the TFT. When an organic material, as in this invention, is used as a gate insulation layer or protection film, the organic material comes in contact with a semiconductor material in which a channel layer of the TFT is formed. In this case, an unexpected problem may occur. Conventionally, a chemical vapor deposition (CVD) process has been used for the formation of an insulation film or semiconductor layer. The chemical reaction in the CVD chamber for the formation of SiO_2 as a gate insulation layer is as follows.

$$SiH_4 + 2N_2O = SiO_2 + 2N_2 + 2H_2$$

And the chemical reaction in the CVD chamber for the formation of Si_3N_4, which is mainly used for a protection film is as follows.

$$3SiH_4 + 4NH_3 = Si_3N_4 + 12H_2$$

Finally, the chemical reaction for the formation of silicon is as follows.

$$SiH_4 = Si + 2H_2$$

When the insulation film or protection film that includes silicon is formed on a silicon semiconductor layer, the insulation film or protection film is formed by a similar CVD process to that in the formation of the semiconductor layer. Thus, chemical bondings are created at the interface between the film and the silicon semiconductor layer. However, an organic material, which is spin coated

on the surface of the silicon semiconductor, does not provide chemical bondings at the interface. This causes the following two problems.

The first problem is detachment of the organic film from the semiconductor layer. The second problem is a charge trap phenomenon; traps for electric charges are created at the interface, causing unstable TFT characteristics. In general, it is desirable for the carriers to be electrons of negative charges rather than holes of positive charges, since a TFT for an LCD requires a fast response time. Therefore, a p-type or intrinsic semiconductor is used for the channel layer and an n+ semiconductor is used for the dopant to the source or drain electrode. When a positive voltage is applied to the gate, electrons are induced in the semiconductor layer adjacent to the gate insulation layer and an n-type channel is formed. Then, electrons in the source electrode can move toward the drain electrode through the channel layer. Here, the source- drain current is determined by the gate voltage. On the other hand, when an organic material is used for the gate insulation layer, there are electron traps on the surface of the semiconductor layer due to the free bond radicals between the organic material and the semiconductor material. This causes electrons to be trapped in the electron traps when an n-type channel is formed. These electrons remain on the surface of the semiconductor layer even when the applied voltage is released and the TFT is in the OFF state. Thus, when the TFT is turned on again, the TFT becomes the ON state even at a relatively low applied voltage due to the trapped electrons. Thus, the ON characteristic curve of the TFT moves toward the negative direction of the gate voltage (FIGs. 7A and 7B). Therefore, to eliminate such problems, a certain treatment is necessary for the interface between the organic material and the semiconductor layer.

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

In the present embodiment, an organic material derived from benzocyclobutene (BCB) is selected for a gate insulation layer and/or protection

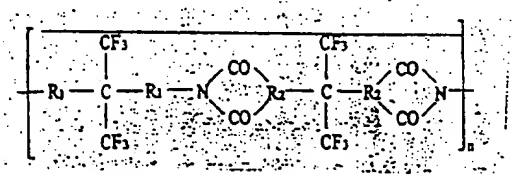
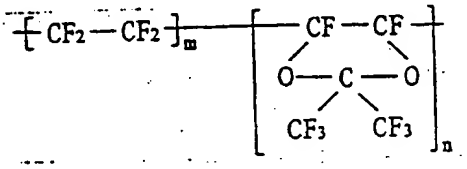
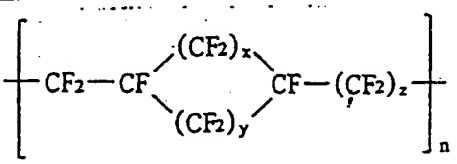
film. BCB reveals superior properties to those of polyimide as shown in Table 1.

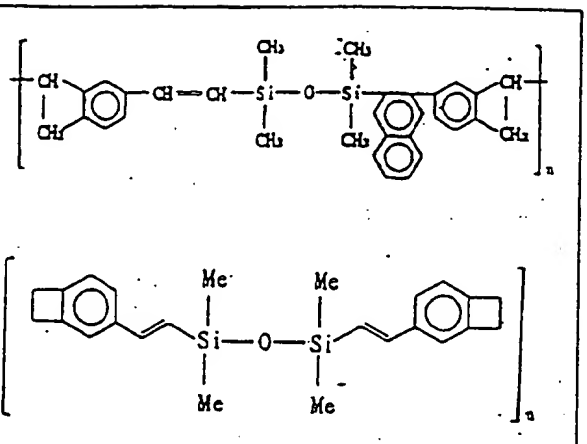
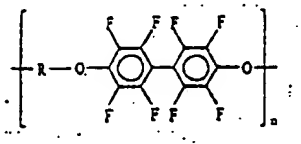
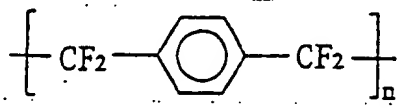
Table 1. Comparison of various properties between BCB and polyimide.

Property	BCB	Polyimide
Dielectric constant	2.7	3.4 - 3.8
Intrinsic resistivity (Ω °cm)	10^{19}	10^{15}
Water contained (%)	0.25	1.7
Treatment temperature (°C)	200 - 250	350 - 400
Compatibility to ITO	Good	Poor

An organic material derived from PFCB can also be used for an LCD, which has superior properties of dielectric constant of 2.3 to 2.4 and the Degree of Planarization (DOP) of more than 90%. An organic material such as fluorinated polyimide, teflon, cytop, fluoropolyarylether, or fluorinated para-xylene, all of which have a dielectric constant less than 3, may also be used for the manufacture of an LCD. Table 2 shows the specific dielectric constants of these materials.

Table 2. Dielectric Constant of organic materials used for an LCD in this invention.

Organic material	Dielectric constant	Structure
Fluorinated polyimide	2.7	
Teflon	2.1 - 1.9	
Cytop	2.1	

BCB	2.7	
Fluoro-poly-arylether	2.6	
Fluorinated para- xylene	2.4	

First Preferred Embodiment

Referring now to FIGs. 10A to 10G, the first preferred embodiment of the present invention will be described. A first metal, such as Cr, Ti, Al, Ti-Mo, Mo-Ta or Al-TA, is deposited on a transparent glass substrate 111 (1000 to 2000 Å thick). The film is patterned to form a gate bus line and a gate electrode 113 as shown in FIG. 10A. Then, the overall surface is coated with an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para- xylene, PFCB, or BCB to form a gate insulation layer 157 (about 4000 Å thick).

Here, the thickness of the organic film on the gate electrode 113 is about 2000 Å but that on the substrate is about 4000 Å as shown in FIG. 10B. As a result, the organic film has a smooth surface. Thus, problems such as line disconnection and/or short circuit, which arise during the deposition of a thin film on a stepped surface, can be prevented by this organic coating method of the present invention. Moreover, even though the gate insulation layer on the gate electrode is relatively thin, the organic insulation layer has a sufficient insulation property. This is because the resistivity of the organic material is higher than that of conventional inorganic materials for the gate insulation layer. On the other hand, the TFT cannot work efficiently if the dielectric constant of the gate insulation layer is so low that field effect of the TFT does not occur properly. However, the application of the organic film rather than an inorganic film on a gate electrode does not affect the function of a TFT. This is because the thickness of the organic film on the TFT is reduced to compensate the low dielectric constant of the organic film.

Next, an amorphous semiconductor material and an impurity- doped semiconductor material are deposited on the gate insulation layer 157 and patterned to form a semiconductor layer 119 and an impurity-doped semiconductor layer 121 (FIG. 10C). Then, a second metal, such as Cr, Mo, Ti, Cr alloy, or Al alloy, is deposited on the impurity-doped semiconductor layer 121 and patterned to form a signal bus line 125, a source electrode 123, and a drain electrode 127. The exposed portion of the impurity-doped semiconductor layer 121 is then removed (FIG. 10D) by using the patterned electrodes (123 and 127) as a mask. Here, the source and drain electrodes make an ohmic contact with the impurity-doped semiconductor layer 121. Subsequently, a protection film 159 is deposited on the overall surface as shown in FIG. 10E. The protection film is made of an organic material such as fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xlyene, PFCB, or BCB. A

contact hole is formed in the protection film over the drain electrode 127. Then, ITO is deposited on the overall surface and patterned to form a pixel electrode 131, which is in contact with the drain electrode 127 through the hole, as shown in FIG. 10F.

FIG. 8 is a perspective view of the intersection between gate and signal bus lines. When the gate insulation layer 157 is coated on the gate bus line 115, and the signal bus line 125 is deposited on the gate insulation layer 157, the stepped profile due to the gate bus line 115 is not reflected on the surface of the gate insulation layer 157. Thus, the pixel electrode formed on the protection film does not have any short circuit, even when it is formed to overlap signal bus lines or gate bus lines. Moreover, due to the low dielectric constant of the organic material, the method does not require spaces or gaps between pixel electrodes and gate and signal bus lines. Consequently, as shown in FIG. 9, it is possible to form a wider pixel electrode than that in a conventional method. This yields an improved aperture ratio. The aperture ratio can be improved as much as 80%. Therefore, a high quality contrast can be achieved without a light shielding film.

In the manufacture of an LCD described above, the impurity- doped semiconductor layer is removed during the etching process of the source and drain electrodes. During the etching process of the impurity-doped semiconductor layer, the semiconductor layer may also be etched undesirably. An etch stopper layer 135 of an inorganic material may be formed on the semiconductor layer in order to prevent such an over- etching (FIG. 10G). This introduces an additional stepped shape in the TFT structure. In this case, the application of an organic material as a protection film is also advantageous.

Second Preferred Embodiment

Referring now to FIGs: 11A to 11F, the second preferred embodiment of the present invention will be described. A metal such as Cr, Mo, Ti, Cr alloy,

or Al alloy is deposited on a transparent glass substrate 111, followed by the deposition of an impurity-doped amorphous semiconductor material. The resultant two films are patterned together to form a signal bus line 125, a source electrode 123, a drain electrode 127, and an impurity-doped semiconductor layer 121, as shown in FIG. 11A. Here, the impurity-doped semiconductor layer 121 makes an ohmic contact with the source and drain electrodes. Then, a semiconductor is deposited and patterned to form a semiconductor layer 119. The exposed portions of the impurity-doped semiconductor layer 121 which are not covered by the semiconductor layer 119 are also removed as shown in FIG 11B. Next, an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyaryether, fluorinated para- xylene, PFCB, or BCB is coated on the overall surface to form a gate insulation layer 157. The use of an organic material with a high planarization property results in a smooth surface on the insulation layer as shown in FIG 11C.

Next, a second metal such as Cr, Ti, Ta, Al, Ti-Mo, Mo-Ta, or Al alloy is deposited on the gate insulation layer 157 and patterned to form a gate bus line and a gate electrode 113, as shown in FIG. 11D. An organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para- xylene, PFCB, or BCB is coated on the overall surface to form a protection film 159, as shown in FIG 11E. A contact hole is formed in the protection and insulation layers over the drain electrode 127. Then, ITO is deposited and patterned to form a pixel electrode 131, as shown in FIG. 11F.

Third Preferred Embodiment.

Referring now to FIGs. 12A to 12F, the third preferred embodiment of the present invention will be described. A polycrystalline intrinsic semiconductor is deposited on a transparent substrate 111, followed by deposition of an impurity-doped semiconductor material. The resultant two films are patterned

together to form a semiconductor layer 119 and an impurity-doped semiconductor layer 121, as shown in FIG. 12A. Subsequently, a first metal, such as Cr, Mo, Ti, or Cr-Al, is deposited and patterned to form a signal bus line 125, a source electrode 123, and a drain electrode 127. Then, the exposed portion of the impurity-doped semiconductor layer 121 is removed using the source and drain electrodes as a mask (FIG. 12B). The impurity-doped semiconductor layer 121 makes an ohmic contact with the source and drain electrodes. Next, an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB is coated on the overall surface to form a gate insulation layer 157, as shown in FIG. 12C.

A second metal such as Cr, Ti, Ta, Al, Ti-Mo, or Al-Ta is deposited on the gate insulation layer 157 and patterned to form a gate bus line and a gate electrode 113, as shown in FIG. 12D. Here, the gate insulation layer 157 may be etched to be the same pattern as the gate electrode. Next, an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB is coated on the overall surface to form a protection film 159, as shown in FIG. 12E. A contact hole is formed in the protection film 159 and the gate insulation layer 157 over the drain electrode 127. Then, ITO is deposited and patterned to form a pixel electrode 131, as shown in FIG. 12F. The pixel electrode 131 is electrically connected to the drain electrode 127 through the contact hole.

Fourth Preferred Embodiment

Referring now to FIGs. 13A to 13G, the fourth preferred embodiment of the present invention will be described. A polycrystalline semiconductor material is deposited on a transparent substrate 111 and patterned to form a semiconductor layer 119, as shown in FIG. 13A. In general, there are three methods to form the polycrystalline semiconductor layer. First, a polycrystalline silicon is formed

by depositing an amorphous silicon and annealing it by laser. Second, a polycrystalline silicon is formed by depositing an amorphous silicon and thermally annealing it. Third, a polycrystalline silicon material is directly deposited. Next, an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para- xylene, PFCB, or BCB is coated on the overall surface to form a gate insulation layer 157. Then, a first metal such as Cr, Ti, Ta, Al, Ti-Mo, Mo-Ta, or Al alloy is deposited on the insulation layer and patterned to form a gate bus line and a gate electrode 113, as shown in FIG 13B. The gate electrode is formed to be located at about the center of the semiconductor layer 119. The two edge portions of the semiconductor layer are formed into a first impurity-doped semiconductor layer 121 by injecting impurity-ions into the semiconductor layer 119 using the gate electrode 113 as a mask (dopant concentration 10^{14} to 10^{15} cm^{-3})(FIG. 13C). Then, a photoresist is coated over a certain portion of the first impurity-doped semiconductor layer 121. A second impurity-doped semiconductor layer 121' is then formed by injecting impurity-ion (dopant concentration 10^{16} to 10^{18} cm^{-3}). The part covered by the photoresist is the LDD part with injected impurity-ions having lower density (FIG. 13D).

Alternatively, the step described referring to FIG. 13C may be omitted. In this case, after a photoresist is coated to cover a certain part of the semiconductor layer 119, an impurity-doped semiconductor layer 121' is formed by injecting impurity-ions (dopant concentration 10^{16} to $10^{18}cm^{-3}$). Here, the part covered by the photoresist becomes an offset part.

Next, an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB is coated on the overall surface to form a first protection film 159, as shown in FIG. 13E. First Contact holes are formed in the protection film 159 over the second impurity-doped semiconductor layer 121'. Then, a second

metal such as Cr, Mo, Ti, or Cr-Al is deposited and patterned to form a source electrode 123, a drain electrode 127, and a signal bus line 125, as shown in FIG. 13F. An organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB is coated on the overall surface to form a second protection film 133. ITO is deposited and patterned to form a pixel electrode 131 as shown in FIG. 13G. The pixel electrode 131 is electrically connected to the drain electrode 127 through a second contact hole formed in the second protection film 133.

Fifth Preferred Embodiment

In the above-mentioned first to fourth embodiments, an organic gate insulation layer 157 and/or an organic protection film 159 is in contact with a semiconductor layer 119. In that circumstance, problems such as detachment and charge trap may occur. To solve this problem, an inorganic layer such as silicone oxide or silicone nitride is formed between the semiconductor layer and the organic film. The inorganic materials are deposited by, for example, CVD. This embodiment introduces this inorganic layer in the above-mentioned four embodiments.

FIGs. 14A to 14D show the cases of manufacturing an inverse staggered TFT. After forming a gate insulation layer 157 of an organic material, a first inorganic film 177 is formed by depositing silicone oxide or silicone nitride, for example, prior to the deposition of a semiconductor layer 119. This eliminates problems such as detachment and electron trap which could occur at the interface between the organic gate insulation layer 157 and the semiconductor layer 119, as shown in FIG. 14A.

Alternatively, after forming source electrode 123 and a drain electrode 127, a second inorganic film 179 is deposited prior to a formation of an organic protection film 159 (FIG. 14B). In this case, problems such as detachment and charge trap, which could arise at the interface between a semiconductor layer and

organic protection film, can be prevented. Moreover, when both the gate insulation layer 157 and the protection film 159 are formed by organic materials, it is evident that a better result can be obtained by forming both the first and second inorganic films 177 and 179 (FIG. 14C).

When there is an etch stopper layer in an inverse staggered type TFT, the problems such as electron trap do not occur at the interface between a semiconductor layer 119 and an organic protection film 159, since the etch stopper layer is formed from an inorganic material. Thus, in the etch stopper case including the etch stopper layer 135, it is sufficient to form the first inorganic film between the semiconductor layer 119 and the gate insulation layer 157 (FIG. 14D).

FIG. 14E shows the case of manufacturing a staggered type TFT. After forming a semiconductor layer 119 on a substrate 111, a first inorganic film 177 is deposited prior to the formation of an organic insulation layer 157. This eliminates problems such as detachment and electron trap which could occur at the interface between the gate insulation layer 157 and the semiconductor layer 119.

FIG. 14F shows the case of manufacturing a coplanar type TFT. After forming semiconductor layer 119 and the source and drain electrodes 123 and 127, a first inorganic film 177 is deposited prior to the formation of an organic gate insulation layer 157. This eliminates problems such as detachment and electron trap which could occur at the interface between the gate insulation layer 157 and the semiconductor layer 119.

FIG. 14G shows the case of manufacturing a self-aligned coplanar type TFT. After forming a semiconductor layer 119, a gate insulation layer 157, and a gate electrode 113, a first inorganic film 177 is deposited. In this case, it is not necessary for the gate insulation layer 157 to be formed of an organic material, since the stepped profile due to the structure of the self-aligned

coplanar TFT is independent of planarization property of the gate insulation material. Thus, if an organic material is not used for the gate insulation layer 157, an inorganic film between a gate insulation layer 157 and semiconductor layer 119 is not necessary. In this case, only the first inorganic film 177 is necessary at the interface between the organic protection film 159 and the impurity-doped semiconductor layer 121'.

Sixth Preferred Embodiment

In an ITO on passivation (IOP) structure, in which a pixel electrode 131 is formed on a protection film 159 , an additional third inorganic film 181 may be formed in order to improve an adhesion property between the pixel electrode 131 and the organic protection film 159. FIGs. 15 and 16 illustrate such structures including the third inorganic film 181 on the protection film in the various types of TFT structures. These structures produce a stable interface between the pixel electrode 131 and the protection film 159.

FIG. 15A shows inverse staggered TFT having the third inorganic film 181 between the protection film 159 and the pixel electrode 131.

FIG. 15B shows an inverse staggered TFT, with etch stopper layer 135, having the third inorganic film 181 between the protection film 159 and the pixel electrode 131.

FIG. 15C shows a staggered TFT, having the third inorganic film 181, between the protection film 159 and the pixel electrode 131.

FIG. 15D shows a coplanar TFT, having the third inorganic film 181, between the protection film 159 and the pixel electrode 131.

FIG. 15E shows a self-aligned coplanar TFT, having the third inorganic film 181, between the protection film 133 and the pixel electrode 131.

Additionally FIG. 16A shows inverse staggered TFT having the third inorganic film 181 between the protection film 159 and the pixel electrode 131, with the first inorganic film 177 between the gate insulation layer 157 and the

semiconductor layer 119.

FIG. 16B shows inverse staggered TFT having the third inorganic film 181, with the second inorganic film 179 deposited prior to a formation of an organic protection film 159.

FIG. 16C shows inverse staggered TFT having the third inorganic film 181, with the first inorganic film 177 and the second inorganic film 179.

FIG. 16D shows inverse staggered TFT having the third inorganic film 181, with the etch-stopper layer 135 and the first inorganic film 177.

FIG. 16E shows staggered TFT having the third inorganic film 181, with the first inorganic film 177 deposited prior to the formation of the organic insulation layer 157.

FIG. 16F shows a coplanar TFT having the third inorganic film 181, with first inorganic film 177 deposited prior to the formation of the organic insulation layer 157.

FIG. 16G shows a self-aligned coplanar TFT having the third inorganic film 181, with first inorganic film 177, between second protection film 133 and the pixel electrode 131.

Seventh Preferred Embodiment

FIGs. 17A to 17D show the cases where the gate insulation layers are made of an organic material and the protection films are made of an inorganic material. FIG. 17A shows inverse staggered TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material.

FIG. 17B shows inverse staggered TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material, with the etch stopper layer 135.

FIG. 17C shows staggered TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material.

FIG. 17D shows a coplanar TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material.

Additionally, as the fifth preferred embodiment, an intermediate film comprising an inorganic material is formed between the gate insulation layer 157 and the semiconductor layer 119.

FIG. 18A shows inverse staggered TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material, with the first inorganic film 177.

FIG. 18B shows inverse staggered TFT, where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material, with the first inorganic film 177 and etch stopper layer 135.

FIG. 18C shows a staggered TFT where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material, with the first inorganic film 177.

FIG. 18D shows a coplanar TFT, where the gate insulation layer 157 is made of an organic material and the protection film 139 is an inorganic material, with theprotection films 159 are made of an organic material and the gate insulation layers 157 are made of an inorganic material.

FIG. 19A shows inverse staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material.

FIG. 19B shows inverse staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the etch stopper layer 135.

FIG. 19C shows staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material.

FIG. 19D shows coplanar TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material.

FIG. 19E shows self-aligned coplanar TFT, where the first protection film 159 is made of an inorganic material and the second protection film 133 is an organic material, wherein the gate insulation layer 157 can be either an inorganic or organic material because it does not influence the level-difference.

FIG. 19F shows self-aligned coplanar TFT, where the first protection film 159 is made of an organic material and the second protection film 133 is made of an inorganic material, wherein the gate insulation layer 157 can be either an inorganic or organic material because it does not influence the level-difference.

Additionally, in an ITO on passivation structure, in which a pixel electrode 131 is formed on a protection film 159, third inorganic film 181 may be formed in order to improve an adhesion property between the pixel electrode 131 and the organic protection film 159.

FIG. 20A shows inverse staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the third inorganic film 181 between the pixel electrode 131 and the organic protection film 159.

FIG. 20B shows inverse staggered TFT having an etch stopper layer 135, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the third inorganic film 181.

FIG. 20C shows staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the third inorganic film 181.

FIG. 20D shows coplanar TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the third inorganic film 181.

FIG. 20E shows self-aligned coplanar TFT, where the first protection film 159 and the gate insulation layer 157 are made of an inorganic material and the second protection film 133 is an organic material, with the third inorganic

film 181 between the second organic protection film 133 and the pixel electrode 131.

Specially, in the cases of invert staggered TFT, the semiconductor layer 119 should be contacted with the protection film 159 comprising an organic material. So, the second inorganic film 179 may be formed prior to a formation of the organic protection film 159.

FIG. 21A shows a inverse staggered TFT without etch stopper layer, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the second inorganic film 179 deposited prior to a formation of the organic protection film 159.

FIG. 21B shows a inverse staggered TFT, where the protection film 159 is made of an organic material and the gate insulation layer 157 is an inorganic material, with the second inorganic film 179 and the third inorganic film 181.

In the present invention, an organic material was used as an insulation and/or protection film in an LCD. Thus, an LCD having superior performance is obtained compared to a conventional LCD which uses silicon oxide or silicon nitride for the insulation and/or protection film.

The superior insulation property is obtained by using an organic material such as, or an organic material derived from, fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB, for a gate insulation layer. Also, a smoother surface of a protection film is obtained by using an organic material such as fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB, or BCB, on a stepped surface due to the multilayered structure of the TFT. It also becomes possible to form a wider pixel electrode than in a conventional method, improving an aperture ratio. Moreover, an orientation film, which determines an initial liquid crystal orientation, becomes smoother, allowing uniform rubbing of the orientation film. Accordingly, an LCD with a superior performance to a

conventional LCD can be manufactured by the present invention.

It will be apparent to those skilled in the art that various modifications and variations can be made in a liquid crystal display and a method for manufacturing the same of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

CLAIMS

1. A transistor substrate for a liquid crystal display comprising:
a substrate;
a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer; and
a protection film over the transistor, the protection film including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

2. The transistor substrate according to claim 1, further comprising:
a gate bus line connected to the gate of the transistor;
a signal bus line connected to one of the source and drain of the transistor; and
pixel electrode over the protection film, the pixel electrode being connected to another one of the source and the drain of the transistor, wherein at least one of the gate bus line and signal bus line is located under the protection film and the pixel electrode overlaps at least a portion of one of the gate bus line and the signal bus line located under the protection film.

3. The transistor substrate according to claim 1, further comprising an intermediate layer between the protection film and the transistor.

4. The transistor substrate according to claim 2, further comprising an intermediate layer between the protection film and the transistor.

5. The transistor substrate according to claim 2, further comprising an intermediate layer between the protection film and the pixel electrode.

6. A transistor substrate for a liquid crystal display comprising:
a substrate; and
a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulating layer, the gate insulating layer including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

7. The transistor substrate according to claim 6, further comprising:
a gate bus line connected to the gate of the transistor;
a signal bus line connected to one of the source and the drain of the transistor; and
a pixel electrode connected to another one of the source and the drain of the transistor, the pixel electrode overlapping at least a portion of one of the gate bus line and the signal bus line.

8. The transistor substrate according to claim 6 or 7, further comprising an intermediate layer between the gate insulation layer and the semiconductor layer.

9. A transistor substrate for a liquid crystal display comprising:
a substrate;
a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulating layer, the gate insulating layer including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para- xylene, PFCB or BCB; and
a protection film over the transistor, the protection film including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

10. The transistor substrate according to claim 9, further comprising:
a gate bus line connected to the gate of the transistor;
a signal bus line connected to one of the source and the drain of the transistor; and
a pixel electrode over the protection film, the pixel electrode being connected to another one of the source and the drain of the transistor, wherein at least one of the gate bus line and the signal bus line is located under the protection film and the pixel electrode overlaps at least a portion of one of the gate bus line and the signal bus line located under the protection film.

11. The transistor substrate according to claim 9 or 10, further comprising an intermediate layer between the protection film and the transistor.

12. The transistor substrate according to claim 9, 10 or 11, further comprising an intermediate layer between the gate insulation layer and the semiconductor layer.

13. The transistor substrate according to claim 10, further comprising an intermediate layer between the protection layer and the pixel electrode.

14. A method for manufacturing a transistor substrate for a liquid crystal display, the method comprising the steps of:
forming a transistor over the substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer; and
forming a protection film over the transistor, the protection film including a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

15. The method for manufacturing a transistor substrate according to claim 14, the method further comprising the steps of :
forming a gate bus line connected to the gate of the transistor;
forming a signal bus line connected to one of the source and the drain of the transistor; and
forming a pixel electrode over the protection film, the pixel electrode being connected to another one of the source and the drain of the transistor,
wherein at least one of the gate bus line and the signal bus line is formed under the protection film; and
the pixel electrode overlaps at lest a portion of one of the gate bus line and the signal bus line located under the protection film.

16. The method for manufacturing a thin film transistor substrate according to claim 14 or 15, the method further comprising the step of forming an intermediate layer between the protection film and the transistor.

17. The method for manufacturing a transistor substrate according to claim 14, 15 or 16, the method further comprising the step of forming an intermediate layer over the protection layer.

18. A method for manufacturing a transistor substrate for aliquid crystal display, the method comprising the steps of:
forming a transistor on a substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer, wherein the gate insulation layer includes a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

19. The method for manufacturing a transistor substrate according to claim

18, the method further comprising the steps of:
forming a gate bus line connected to the gate of the transistor;
forming a signal bus line connected to one of the source and the drain of the transistor; and
forming a pixel electrode connected another one of the source and the drain of the transistor, wherein the pixel electrode overlaps at least a portion of one of the gate bus line and the signal line.

20. The method for manufacturing a transistor substrate according to claim 18 or 19, the method further comprising the step of forming an intermediate layer between the gate insulation layer and the semiconductor layer.

21. A method for manufacturing a transistor substrate for a liquid crystal display, the method comprising the steps of:
forming a transistor on a substrate, the transistor having a gate, a source, a drain, a semiconductor layer, and a gate insulation layer, wherein the gate insulation layer includes a material derived from fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB; and
forming a protection film over the transistor, the protection film including a material derived from at least one of fluorinated polyimide, teflon, cytop, fluoropolyarylether, fluorinated para-xylene, PFCB or BCB.

22. The method for manufacturing a transistor substrate according to claim 21, the method further comprising the steps of:
forming a gate bus line connected to the gate of the transistor;
forming a signal bus line connected to one of the source and the drain of the transistor; and
forming a pixel electrode over the protection film, the pixel electrode being

connected to another one of the source and the drain of the transistor,
wherein at least one of the gate bus line and signal bus line is formed under the protection film; and
the pixel electrode overlap at least a portion of one of the gate bus line and the signal bus line located under the protection film.

23. The method for manufacturing a transistor on a substrate according to claim 21 or 22, the method further comprising the steps of forming an intermediate layer between the protection film and the transistor.

24. The method for manufacturing a transistor on a substrate according to claim 21, 22 or 23, the method further comprising the steps of forming an intermediate layer between the gate insulation layer and the semiconductor layer.

25. The method for manufacturing a transistor on a substrate according to claim 22, the method further comprising the step of forming an intermediate layer between the protection layer and the pixel electrode.

26. A semiconductor device insulating layer, wherein the insulating layer comprises an organic material.

27. An insulating layer according to Claim 26, wherein the insulating layer comprises fluorine-containing organic polymer.

28. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from fluorinated polyimide.

29. An insulating layer according to Claim 26, wherein the insulating layer

comprises a material derived from teflon or a compound of like chemical composition.

30. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from cytop or a compound of like chemical composition.

31. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from fluoropolyarylether.

32. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from fluorinated para-xylene.

33. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from PFCB.

34. An insulating layer according to Claim 26, wherein the insulating layer comprises a material derived from BCB or other polymer comprising benzocyclobutene units.

35. An insulating layer according to any one of claims 26 to 34, wherein the insulating layer also comprises an inorganic material.

36. A semiconductor device insulating layer having, or being derived from, any one of the respective chemical structures shown in Table 2 appearing hereinbefore.

37. A semiconductor switching device for a liquid crystal display, wherein the

gate insulation layer and/or the protection layer comprise an insulating layer according to any one of Claims 26 to 36.

38. A thin film transistor for a liquid crystal display, wherein the gate insulation layer and/or the protection layer comprise an insulating layer according to any one of Claims 26 to 36.

39. A method of manufacturing a semiconductor device, comprising spin coating an insulating layer according to any one of claims 26 to 36.

40. A transistor substrate, a method for manufacturing a transistor substrate, a method of manufacturing a semiconductor device, a semiconductor device insulating layer, a semiconductor device and/or a thin film transistor substantially according to any one of the first to eighth embodiments hereinbefore described and illustrated.

41. A transistor substrate, a method for manufacturing a transistor substrate, a method of manufacturing a semiconductor device, a semiconductor device insulating layer, a semiconductor device and/or a thin film transistor substantially as hereinbefore described with reference to and/or as illustrated in any one of or any combination of Figs. 8 to 21B of the accompanying drawings.

The Patent Office

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Application No:	GB 9706354.9	**Examiner:**	SJ Morgan
Claims searched:	1-41	**Date of search:**	9 June 1997

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KCAA,KJAD); G5C(CHG)

Int Cl (Ed.6): H01L; G02F

Other: Online:WPI, JAPIO, CLAIMS, EDOC, INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	WO 95/31823 A1 (ELECTROTECH)	26
X	WO 95/17006 A1 (NATIONAL SEMICONDUCTOR)	26
X	US 5 468 685 (MITSUBISHI)	26
X	Research Disclosure 38337, 10/3/96, (ANONYMOUS)	1-27, 33, & 36-39
X	Patent Abstracts of Japan, Section C, Section No 307, Vol 9, No 247, Pg 114, 3/10/85 & JP 60-104129A (HITACHI). See abstract.	26-28
X	Patent Abstracts of Japan, Section P, Section No. 87, Vol. 05, No. 173, Pg. 45, 5/11/81 & JP56-100350A (MAKOTO). See abstract.	26 & 29

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